DP5 Programmer's Guide

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Note: This document applies to the Amptek DP5, PX5, TB5, DP5G, MCA8000D and products derived from these (X123, Gamma-Rad5).

Table of Contents

1 Change List

DP5 Programmer's Guide B0 is released with firmware version FW6.09.02, FPGA version FP6.13, and Visual Basic Demo v2.87.

1.1 Programmer's Guide Rev B0 (this document)

Current as of FW6.09.02/FP6.13
Support for DP5 Rev D
Significant enhancements to 16-bit List Mode (see section 4.2.22)
Cleaned up section 2, on uploading firmware
The sense of GATE for MCA8000D was reversed in section 5.1.19 – documentation was fixed, and a note was added mentioning how to change the sense, if that should be desired
Corrected MCA Source description for MCAS command (see section 5.1.31)
Added notes under PAPZ (for HPGe) and RESL relating to using RESL to reject overrange events (see sections 5.1.37 and 5.1.49)

1.2 Programmer's Guide Rev A8

Current as of FW6.08.04/FP6.10
Fixed typo in section 4.2.19 – had incorrect PIDs for 'Text Configuration Readback' request packet
The 'Status packet' response packet has a few additions (section 4.2.1)

1.3 Programmer's Guide Rev A7

Current as of FW6.08.00/FP6.06 (see change list below)
MCA8000D documentation added
Equation for 'DP5 board temp (raw)' in diagnostic packet (Section 4.2.18) was in error. Fixed.
Added note to Text Configuration packet about delay caused by FLASH write
Section 6.3 is new (Sequential Buffering)
A note was added to Section 3 describing that in the DP5G, Ethernet is disabled at boot in the presence of USB or RS232
Section 3.1.2 was added, listing WinUSB GUIDs
Section 4.1 includes new Request Packets
The 'Status packet' response packet has a few additions (section 4.2.1)
New "Text Configuration (without saving to nonvolatile memory)" command was Request Packet was added (Section 4.1.20)

1.4 Programmer's Guide Rev A6

Current as of FW6.06.06/FP6.00

1.5 Programmer's Guide Rev A5

Section 6 is new.

Describes FW releases
Current as of FW6.06.05/FW5.13
Section 3.1.1 mentions that the WinUSB driver is now available via Windows Update.
Section 3.1.2 adds a discussion of DHCP, and how to set a fixed IP address.
Documentation for List-mode operation (see sections 4.1.13, 4.1.20, 4.1.39, 4.2.22, 4.3.15, 5.1.12, 5.1.65, and 6.1)

1.6 Programmer's Guide Rev A4

Added transfer times (section 3.4)
New commands and packet types are listed below, and in their corresponding sections
Current as of FW6.06.00/FW5.11

1.7 FW6.09.02/FP6.13

IF UPGRADING FROM FW6.07.04 OR EARLIER, FW7.00.01 MUST BE LOADED PRIOR TO UPGRADING TO THIS VERSION!!!
This version (or later) is required if upgrading a DP5 Rev D from FW5 to FW6

1.8 FW6.09.01/FP6.13

IF UPGRADING FROM FW6.07.04 OR EARLIER, FW7.00.01 MUST BE LOADED PRIOR TO UPGRADING TO THIS VERSION!!!
Bug fix: Fast threshold defaulted to full-scale at power-up, if Auto fast threshold was used without subsequently commanding a fixed fast threshold. Fixed – now reverts to last commanded fast threshold.

1.9 FW6.09.00/FP6.12

IF UPGRADING FROM FW6.07.04 OR EARLIER, FW7.00.01 MUST BE LOADED PRIOR TO UPGRADING TO THIS VERSION!!!
Support for DP5 Rev D – must use this version or later; different GAIA settings, ECO byte in status packet
DMCA: [with FP1.08] ECO=1 inverts the sense of the GATE signal; it was discovered this documentation specifies the opposite from how the MCA8000D actually performs.
DP5G/TB-5 support for CLYC scintillator [ECO=2]

1.10 FW6.08.06/FP6.11

IF UPGRADING FROM FW6.07.04 OR EARLIER, FW7.00.01 MUST BE LOADED PRIOR TO UPGRADING TO THIS VERSION!!!
RTDS range doubled to 3187%
DMCA: Improved performance with bipolar pulses [with FP1.08]
THSL setting of 0 no longer allowed; defaults to 0.012% (1 ch out of 8192)
PX5: Allow RESL in conjunction with PAPZ to lockout processing after overrange events, which can cause spectrum artifacts. (In this context, RESL logic detects overrange events rather than resets.) Additional support for deadtime correction in 16-bit List Mode (see section 4.2.22)

1.11 FW6.08.04/FP6.10

IF UPGRADING FROM FW6.07.04 OR EARLIER, FW7.00.01 MUST BE LOADED PRIOR TO UPGRADING TO THIS VERSION!!!
Fixed rounding error with HPGe PAPZ command readback (which was introduced in FW6.07.05)
Fixed SYNC command readback
New AU34 command
Fixed 0.1% timebase error in 16-bit List Mode

1.12 FW6.08.03/FP6.09

IF UPGRADING FROM FW6.07.04 OR EARLIER, FW7.00.01 MUST BE LOADED PRIOR TO UPGRADING TO THIS VERSION!!!
RTD timing improved for faster TPFA settings introduced in FW6.07.05/FP6.04
DPG/TB5: RESL can be used for gamma-ray rejection starting in FP6.09

1.13 FW6.08.02/FP6.07

IF UPGRADING FROM FW6.07.04 OR EARLIER, FW7.00.00 MUST BE LOADED PRIOR TO UPGRADING TO THIS VERSION!!!
LMMO command added for list mode, to improve ability to calculate deadtime (see sections 4.2.22, 5.1.28 and 6.1)
Streaming bug fix: streaming amplitude was a bit off at peaking times of 1.6uS or faster (at 80MHz)

1.14 FW6.08.01/FP6.06

IF UPGRADING FROM FW6.07.04 OR EARLIER, FW7.00.00 MUST BE LOADED PRIOR TO UPGRADING TO THIS VERSION!!!
Support for new product 'TB-5 Digital Tube Base'

'SCTC' new command for DP5G and TB5
FP6.06 fast channel improved to reduce spurious fast-channel counts for DP5G and TB-5

1.15 FW6.08.00/FP6.06

IF UPGRADING FROM FW6.07.04 OR EARLIER, FW7.00.00 MUST BE LOADED PRIOR TO UPGRADING TO THIS VERSION!!!
Fixed bug in MCA8000D MCS timebase
Improved BLR initialization during reconfiguration
New Text Configuration Request Packet which skips the Flash write (Section 4.1.20)
New sequential buffering feature (Section 6.3)

1.16 FW6.07.05/FP6.04

IF UPGRADING FROM FW6.07.04 OR EARLIER, FW7.00.00 MUST BE LOADED PRIOR TO UPGRADING TO THIS VERSION!!!
More 'TPFA' (fast channel peaking time) options: 50, 100, 200, 400 or 800nS (80MHz); 200, 400, 800, 1600 or 3200nS (20MHz)
Default MCS Timebase ('MCST') changed to 1S; was 0, which is invalid
'Comm test – Streaming Test Mode' request packet added (Section 4.1.46)
'RESPER' (detector reset period) option added to 'GPIN' command

1.17 FW6.07.04/FP6.03

'RESL' (Reset Lockout) can now be set with 1uS precision, rather than rounding to a power-of-2.
PX5-HPGe: HV is always turned off at power-up
Windows 8 USB descriptors were added, which may utilize WinUSB without having to install a USB driver (See section 3.1 – it is presently unclear if these actually work as Microsoft advertises.)

1.18 FW6.07.02/FP6.01

'RTDS' command default changed from 0 to 2 (0 was an invalid setting)
GATE bit was in incorrect bit in status packet – fixed
'Option PA' calibration request packet, response packet and ACK packet for MCA8000D

1.19 FW6.06.07/FP6.01

GATE state added to status packet
Additional PX5 HPGe support added

1.20 FW6.06.06 / FP6.00

'Streaming' feature added; 'STREAM' option added for 'AUO2' command (See section 6.2)
Additional fine-gain precision added
Increased ping data buffer size from 32 to 56 bytes, to handle default Linux ping size
DP5G: added support for Gammarad AD592 temperature sensor via PCG ADC; scintillator temperature shows up as 'detector temperature' in Status Packet
Added 16-bit List-mode capability ('SYNC=NOTIMETAG') (See sections 4.2.22, 5.1.65 and 6.1)
Added List-mode configuration byte in Status Packet (Section 4.2.1)

1.21 FW6.06.05 / FP5.13

Default static IP address changed from 255.255.255.255 to 192.168.1.10
PX5: Power button changed from Green/Amber (+HV) or Red/Amber (-HV) to Green/Off and Red/Off during acquisition. (Still solid Green or Red with acquisition stopped)
List-mode support (requires FP5.13) [CLKL and SYNC commands; Request packet PIDs 3/9 and 0xF0/0x16; Response packet PIDs 0x82/0x0A and 0x82/0x0B; ACK PID 0xFF/0x10]
Fixed RTDS rounding error

1.22 FW6.06.04

PX5: added support for HPGe HVPS option (HVSE and PAPS commands; Status packet)
New uC/FPGA upload packet types to improve reliability over Ethernet
Erased/uninitialized/corrupt FPGA will report FP15.15 (i.e. 0xFF)
DP5/PX5: Ethernet UDP socket is no longer closed when USB VBus is detected, i.e. when USB is connected

1.23 FW6.06.03

Changed input offset default values for "INOF=DEF" to accommodate PX5 front end
DPG: Ethernet UDP socket is no longer closed when USB VBus is detected, i.e. when USB is connected

1.24 FW6.06.02

Fixed SOFF command readback bug for -1 < SOFF < 0
PX5: fixed bug with PAPS command readback (read back 8.5 when set to 5)

1.25 FW6.06.01

PX5: added HV polarity to status packet

1.26 FW6.06.00 / FP5.11

Channel numbers were changed to start with channel 0, not channel 1, to be consistent with industry standards. This affects the following text commands: MCSL, MCSH, PRCL, PRCH, SCAL, SCAH,

TLLD. The data format in the spectrum response packets is unchanged, but software should interpret the first channel to be channel 0, not channel 1, to be consistent with the above commands.
The fine gain now has a minimum precision of 1 part in 8192. (It was as low as 1 part in 256 in FP5.10.) This allows the 'GAIN' and 'GAIF' to be set with the precision of 1 channel or better.
Calibration of the PX5 and DP5/PC5 HV supplies is supported.
PAPZ (preamp pole-zero) command for PX5.
Fixed RTD; in FP5.09/FP5.10, only worked with TPFA (fast peaking time) of 100nS (80MHz) or 400nS (20MHz).
Added a 'build number' to the firmware version, in byte 37 of the status packet; FW6.06, build 0 is listed as FW6.06.00.
Improved precision of THFA (Fast Threshold) and THSL (Shaped Threshold) commands.
Added input offset gain command ('INOG') for PX5

1.27 FW6.05 / FP5.10

RS232: A 'Gap timer' was added; support for 57.6kbaud and 19.2kbaud was added, in addition to the standard 115.2kbaud. (See section 3.3).
Added 'reboot' bit to status packet, to aid in detecting unexpected reboot/power cycle.

1.28 FW6.04 / FP5.10

UDP receive buffer was expanded to handle 590-byte DHCP response
Fixed THFA readback for unconfigured condition
Fixed 'Unit is Configured' bit in status packet

1.29 FW6.03 / FP5.10

CON1 & CON2 commands for GammaRad (DP5G/PC5G) and PX5

1.30 FW6.02 / FP5.09

Shaped channel peaking times ('TPEA') down to 50nS; Fast channel peaking times ('TPFA') down to 50nS
UDP port inactivity timeout was increased from 5 to 15 seconds

2 Software

2.1 Uploading new firmware

The Firmware Manager application can be downloaded from the Amptek website for use in loading new firmware, changing various calibration settings, or changing the TCP/IP configuration of the device. Firmware Manager can be downloaded from here:

http://www.amptek.com/firmware/firmwaremanager.zip

Firmware Manager works best if it is allowed to access the Internet, in which case it can install the very latest firmware. However, the ZIP file download includes all current firmware files, so they can be manually installed as needed.

Firmware Manager replaces the Firmware Loader and DP5 Loader applications. Firmware Manager can upgrade FW5-based DP5s via RS232, and all other devices via USB, Ethernet or RS232.

2.2 Software Resources

There are a number of resources available to assist in developing an application:

2.2.1 DP5 VB Demo

The DP5 VB Demo can be downloaded from the Amptek website. It is written in Visual Basic 5, and shows how to use WinUSB, Winsock, and the VB Comm control to communicate with a DP5-family device. It handles nearly all packet types; it can upload new firmware and set various calibration values; it supports List Mode, though not at the highest count rates.

http://www.amptek.com/zip/dppsoft_3.zip

2.2.2 SDK

A Software Development Kit (SDK) is available from the Amptek website. It has C++ and VB examples. Labview and other language examples may also be found on the website. Contact Amptek for more information.

http://www.amptek.com/products/dp5-digital-pulse-processor-software/

3 Interfaces

The DP5 supports three communication interfaces: USB, Ethernet and RS232. Details about the specific interfaces are in the following sections.

Note: Attempting to use multiple interfaces simultaneously can result in unexpected behavior. In firmware prior to FW6.06.04 (DP5/PX5) or FW6.06.03 (DP5G), the Ethernet general UDP socket is disabled whenever the USB port is connected to a live host port. The socket is re-enabled if the USB cable is disconnected, or the host/hub to which the DP5 is physically connected is powered off. In FW6.06.04 (DP5/PX5) or FW6.06.03 (DP5G) and later, this is no longer the case – the UDP port is always open, regardless of whether USB is connected. [This was changed because noise on the unconnected USB connector caused Ethernet dropouts.]

The 'Netfinder' socket remains functional when USB is connected, and the contents of the Netfinder packet indicate if the UDP socket is unavailable because of USB.

The DP5G checks to see if either the USB or RS232 connectors are connected to a live port at power-up. If so, the Ethernet controller is not initialized (to save power), and will remain non-functional until the next power cycle.

3.1 USB

The DP5 family supports 'full-speed' (12Mbps) USB 2.0. Three endpoints are used: the 'control' endpoint (EP0); EP1 IN (for response packets from the DP5 to host PC); and EP2 OUT (for request packets from the host PC to DP5.)

Transfers on EP1 and EP2 are terminated by a 'short packet' (a packet smaller than the max packet size of 64 bytes), or a zero-length packet ('ZLP').

For the DP5, PX5, DP5G, and MCA8000D, the USB Vendor ID (VID) and Product ID (PID) are:
VID: 0x10C4
PID: 0x842A

The DPPMCA application (and DP5 Visual Basic demo) use the WinUSB driver. This is a Microsoft product that is native to Vista and Windows 7 (32- and 64-bit), and installable on WinXP. The Visual Basic demo includes source code, and VC++ classes are available for those wishing to write their own communication software.

3.1.1 Installing the WinUSB Driver

The WinUSB driver has been tested by WinQual and signed for WinXP 32/64, Vista 32/64, and Win7 32/64. It is available via Windows Update, which means that a PC with an Internet connection should be able to install the driver automatically. Directions for manually installing the driver are in the 'WinUSB Driver Installation' folder in the ZIP file.

The ZIP file includes the Microsoft document 'WinUsb_HowTo.docx', which describes the complex process of using Windows' SetupAPI to find the device path, etc. [The VB demo demonstrates this technique, as well as setting pipe policies, opening pipes, sending and receiving data, etc.]

USB.h and USB100.h contain many structures, enums, etc. used by Windows' USB implementation – these files (from DDK6001) are in the ZIP file.

Microsoft's website gives information on how to call the specific WinUSB functions:
http://msdn.microsoft.com/en-us/library/ff540046(v=VS.85).aspx

As of FW6.07.04, Windows 8 USB descriptors have been added, which may allow Win8 to automatically load WinUSB without having to install it. Microsoft's documentation is a bit sketchy on this; it hasn't been tested yet at Amptek.

Win8 descriptors added:

1. An 'OS String Descriptor', to tell Windows that extended feature descriptors are present;
2. An 'Extended Compat ID OS feature descriptor', to tell Windows to use WinUSB; and
3. An 'Extended properties OS feature descriptor', to specify the device's interface GUID.

3.1.2 WinUSB GUIDs

The WinUSB driver for the DP5 family utilizes two GUIDs:

FW6 GUIDs:

Setup Class GUID: {6A4E9A2D-9368-4f01-8E60-B3F9CDBAB5E8}
Interface Class GUID: {5A8ED6A1-7FC3-4b6a-A536-95DF35D03448}

3.2 Ethernet

The DP5 incorporates a 10base-T Ethernet controller and embedded TCP/IP stack to provide Ethernet support via a standard RJ45 jack. The DP5 supports auto-negotiation for half- and full-duplex. Only 10Mbit/s is supported.

PING and ARP are supported. A fixed IP address can be specified, or a dynamic address can be obtained from a DHCP server. (If 'dynamic' is selected, and the DP5 is unsuccessful in obtaining a lease from a DHCP server, it will fall back to its previously-programmed static address.) The IP configuration (fixed/dynamic, IP address, netmask, gateway, and port) can be programmed via any of the DP5 communication interfaces (Ethernet, USB or RS232).

Note: By default, the DP5/PX5/DP5G is configured to use a dynamic IP address. If no DHCP server is present, then the device falls back to the programmed static IP address. Prior to FW6.06.05, if no static IP address was programmed, then the device defaulted to 255.255.255.255, which is not a valid IP address. In this case, if a DHCP server isn't available, then USB or RS232 must be used to assign a valid static IP address. The Firmware Manager application is the preferred way to assign an IP address, although the DP5 VB Demo can also perform this function. In FW6.06.05 and later, if no DHCP server is present and a static IP address hasn't been programmed, the device will default to 192.168.1.10.

In addition, in order to save power, the DP5G powers down the Ethernet controller when a USB or RS232 connection is detected at power-up. This means for a Gammarad (or other devices that can be powered via USB), external power should be applied, and then USB (or RS232) can be connected after approximately five seconds (or more).

Also, for whatever reason, the DP5/PX5/DP5G work poorly via Ethernet when directly connected to a PC's Ethernet port. They work fine if connected to the PC via an Ethernet hub or switch.

3.2.1 Ping

Prior to FW6.06.06, the Ethernet implementation had a 32-byte PING buffer. This worked with Windows, but not with the Linux default ping size of 56 bytes. In FW6.06.06, the PING buffer was increased to accommodate the Linux default ping size. Note that for Linux ping support with older firmware, the Linux default ping size can be overridden.

3.2.2 Ethernet Ports

The DP5 supports two UDP ports for communication: one port is for general communications (fixed at UDP port 10001 in FW6.06, and possibly programmable in later firmware releases), and the other is for device discovery via the Silicon Labs Netfinder protocol (UDP port 3040.)

3.2.3 General UDP Port

By default, the DP5 uses UDP port 10001 for communications. Once a packet exchange has taken place on this port, the socket is 'bound' to the IP address **and source port** of the host it exchanged packets with. Once the socket is bound, packets from other IP addresses will be ignored. After approx. 15 seconds of inactivity on the socket, the socket is reset so that it can once again connect to any IP.

To not allow other hosts to seize control of the DP5, the host can continue exchanging packets so that this timeout does not occur. "Interface keep-alive" Request Packets can be sent periodically, if there is no other periodic traffic, to keep the socket from resetting. Or an "Interface – lock" Request Packet can be sent, in which case the socket will not be reset until power is cycled on the DP5, or the host removes the lock by sending an "Interface keep-alive - allow sharing" or "Interface keep-alive - no sharing" Request Packet.

Broadcast packets can be received by the General UDP Port, which may be useful if multiple DP5s are on a subnet, and synchronization or centralized control is desired. (Request packets such as 'Enable MCA' and 'Clear Spectrum' could be useful as broadcasts.) As of firmware FW6.06, all Request Packets received by the DP5 will generate a Response Packet, which isn't desirable for broadcasts. Future versions of the firmware may use the most significant bit of the PID2 packet ID to indicate a broadcast packet, so that DP5s will be able to suppress Response Packets. Also, a command or Request Packet will be added so that a DP5 can be configured whether to process or ignore broadcast packets. (This will allow some DP5s on a subnet to not participate in broadcasts, if this is desired.)

The existing protocol works over the Internet, but possibly not very well. As it uses raw UDP packets with no sequence numbers, and spectrum packets are large enough that they're split into multiple UDP packets, theoretically the spectrum UDP packets could be received out of sequence, with no way to tell. Eventually, the firmware will have the option to encapsulate each UDP packet within the DP5 packet structure, and use the DP5 packet PIDs as sequence numbers. This should allow the protocol to be more robust when routed over the Internet – the packets will be able to be reordered if they arrive out of sequence, and it will be easier to detect dropped packets.

Timeouts
Generally, the DP5 sends the Response or ACK packet after it has completed the operation specified by the Request Packet. This is usually happens quickly, so that the response is sent with little delay. Since the DP5 always sends a Response or ACK Packet in response to receiving a Request Packet, it may be desirable to use a timeout interval to identify missed packets.

The Visual Basic demonstration software uses a timeout interval of 1000mS by default. However, there are a few packet types which require a longer timeout interval because they may take longer than 1s to execute:

Description	PID1	PID2	LEN MSB	LEN LSB	Recommended Timeout
Request diagnostic data	3	5	0	0	2500mS
Erase FPGA image	0x30	1	0	2	5000mS
Erase uC image #1	0x30	5	0	2	2000mS
Write 512-byte Misc Data	0xF0	0x09	2	0	1000mS

3.2.4 Netfinder UDP port 3040

The DP5 supports the Silicon Labs 'Netfinder' protocol on UDP port 3040. This allows DP5s to be 'discovered' – this is particularly useful if DHCP is used to assign dynamic IP addresses, as the DP5 may have an unknown address.

By broadcasting a Netfinder 'Broadcast Identity Request' to UDP port 3040, the host directs all DP5s that receive the broadcast to respond with an 'Identity Reply', which includes the DP5 serial number, IP

address, MAC address, a text description (if one was programmed), the time the device has been powered, and the status of the interface. The host collects the responses from all the DP5s on the subnet, and can then determine which IP address to access based on DP5 serial number, description, etc.

The 'Broadcast Identity Request' is 6 bytes in size and is defined below. The format of the 'Identity Reply' is also listed below – its size is variable because it contains several variable-length null-terminated strings. Note that the 2nd string, the description, comes from the DP5's 'Misc Data' buffer. If the firmware finds a null-terminated string of 40 characters or less, it will send that as the description string. Otherwise, '(no description)' is used. [Note: the DP5 will not respond to the Netfinder 'standard' 4-byte version of the 'Broadcast Identity Request' as defined by Silicon Labs.]

Note that because UDP packet reception is not guaranteed (packets aren't automatically resent), occasionally not all responses will be received. It may be necessary to send multiple Identity Request packets to receive responses to all units. (This depends on how busy the network is, and how many DP5s are present.) Each subsequent Identity Request should use a different sequence ID – a DP5 will not respond to a repeated Identity Request with the same sequence ID.

Note that while the 'Broadcast Identity Request' packet is normally sent as a UDP broadcast packet (i.e. a destination IP of xxx.xxx.xxx.255), it can also be sent to a specific IP address. Also note that UDP broadcast packets generally are limited to the local subnet, and not routed beyond that.

The 'Interface Sharing Request' format is also listed below. If a Netfinder Identity Reply has indicated that a DP5 is in use, but that sharing is allowed, the host can send the 'Interface Sharing Request' to the Netfinder port of that DP5. The DP5 will use an ACK packet to indicate to its current host that a Sharing Request has been received. If that host wishes to grant the request, it does so by stopping transfers to the DP5's UDP socket, which will allow the socket to reset itself and the new host to gain control of it. [No acknowledgement of the 'Interface Sharing Request' is sent by the DP5 – the host can resend it periodically, and either check the Interface Status in the Netfinder 'Identity Reply', or try sending packets to the DP5 UDP port to see if it responds.]

Broadcast Identity Request – 6 bytes

Offset	0	1	2	3	4	5
Value	0x00	0x00	Random 16-bit sequence ID		0xF4	0x FA

Identity Reply – variable length

Data Offset	Value
0	0x01
1	Ethernet General UDP Port Status: 0 = Interface is open (unconnected); 1 = Interface is connected (sharing is allowed); 2 = Interface is connected (sharing is not allowed); 3 = Interface is locked

	4 = Interface is unavailable because USB is connected
2-3	Replication of Random 16-bit sequence ID received from 'Identity Request'
4-5	Event 1 Days
6	Event 1 Hours
7	Event 1 Minutes
8-9	Event 2 Days
10	Event 2 Hours
11	Event 2 Minutes
12	Event 1 Seconds
13	Event 2 Seconds
14-19	MAC address (MSB…LSB)
20-23	IP Address (MSB…LSB)
24-27	Subnet Mask (MSB…LSB)
28-31	Default Gateway (MSB…LSB)
variable	Null-terminated string: 'Amptek DP5 – S/N ' + serial number 'Amptek PX5 – S/N ' + serial number 'Amptek DP5G – S/N ' + serial number 'Amptek TB-5 – S/N ' + serial number 'Amptek MCA8000D – S/N ' + serial number
variable	Null-terminated string – Description/misc text: "(no description)" if Misc Text isn't programmed; first 41 bytes of Misc Text if programmed
variable	Null-terminated string – Event 1 description: "Time Powered"
variable	Null-terminated string – Event 2 description: "Time on Network"

Interface Sharing Request – 6 bytes

Offset	0	1	2	3	4	5
Value	0x04	0x00	Random 16-bit sequence ID		0xF4	0xFA

3.3 RS232

The RS232 port on the DP5 operates at 115,200 baud, with 1 start bit, 8 data bits, no parity bit, and 1 stop bit. Neither hardware nor software handshaking is used. 57,600 or 19,200 baud operation can be selected; however, selecting these rates will disable the Ethernet port.

The RS232 interface employs a 'gap timer' on its receiver, to aid in synchronization – if the time between consecutive received bytes exceeds 100mS, all buffered bytes are discarded, and the DP5 will resume searching for the sync characters that signal the start of a new packet. No acknowledge packet will be sent to indicate this has occurred.

3.4 Transfer times and data buffering deadtime

In response to a Spectrum (or spectrum + status) request packet, the DP5 will briefly shut off data acquisition, so that it can make a copy of the spectrum memory. When complete, the MCA is re-enabled and the acquisition continues. This 'deadtime' is a function of how many channels are selected (256, 512, etc.) and whether the FPGA is running at 20 or 80MHz. This 'deadtime' will occur each time the spectrum is read out, and this is reflected in the acquisition time; the acquisition timer is stopped during this 'deadtime', while the realtime timer continues to run.

[Note that there is no deadtime penalty for using the ' request spectrum and clear' (or 'request spectrum + status and clear') form of the request packet – the clear function happens simultaneously with the buffering function, and does not add to the 'deadtime'.]

The measured 'deadtimes' are:

# of Channels	20MHz Clock	80MHz Clock
256	228uS	113uS
512	420uS	189uS
1024	804uS	343uS
2048	1.57mS	650uS
4096	3.12mS	1.27mS
8192	6.18mS	2.50mS
Status packet only	31uS	31uS

The USB, Ethernet and RS232 transfer times were measured, using an oscilloscope. The transfer times include the time from when the request packet was started to when the response packet was completed. (i.e. the whole round-trip transfer was measured.)

The transfer times include the 'deadtime' due to buffering, listed above. The transfer times were measured with the 80MHz clock selected, and were measured using the 'Request spectrum + status' request packet. The transfers will run at the same rate with the 20MHz clock, except the 'deadtime' for buffering will be longer. So, for 20MHz timing, use the 80MHz timing, plus the difference between the 20MHz and 80MHz buffering 'deadtime'.

# of Channels	USB (80MHz)	Ethernet (80MHz)	RS232 (115k, 80MHz)	RS232 (57k, 80MHz)
256	2.8mS	11mS	74mS	146mS

512	3.5mS	19mS	140mS	279mS
1024	4.8mS	35mS	273mS	544mS
2048	7.5mS	70mS	538mS	1.07S
4096	12.7mS	134mS	1.07S	2.14S
8192	24.2mS	263mS	2.14S	4.22S

4 Packet Format

All communications with the DP5 follow a request/response format: the host sends a Request Packet to the DP5, and the DP5 returns a Response Packet. The Response Packet sent by the DP5 to the host will be:

a. a packet containing the requested data;
b. an acknowledge (ACK) packet, indicating the request packet was received and interpreted without error (if the request packet is not one for which data is returned);
c. an ACK packet, indicating the request packet contains an error in structure or content;
d. an ACK packet, indicating why the request can't be executed;
e. an ACK packet, indicating that an ASCII command had a unrecognized command field or an invalid parameter field – the command in question will be echoed in the data field of the ACK packet.
f. an ACK packet, indicating the request packet was received and interpreted without error, and a sharing request was received from another computer via Ethernet;

All packets sent to and from the DP5 use the same basic packet format: a 6-byte header, which defines the type and length of the packet, an optional data field, and a 16-bit checksum. For packets sent to the DP5, the optional data field can be up to 512 bytes, for a maximum packet size of 520 bytes. For packets sent by the DP5 to the host PC, the maximum data field size is 32767 for a maximum packet size of 32775 bytes.

Packet Format

Offset	0	1	2	3	4	5	6...5+LEN	6+LEN	7+LEN
Value	0xF5	0xFA	PID1	PID2	LEN_MSB	LEN_LSB	Data (optional, 0-512 bytes)	CHKSUM MSB	CHKSUM LSB

Fields:

Offset 0 & 1: Sync bytes – these fields have fixed values of 0xF5 and 0xFA.

Offset 2 & 3: Packet ID fields 1 & 2 (PID1 & PID2) – these define the meaning of the packet, as summarized in Table 1, Table 2 and Table 3.

Offset 4 & 5: 16-bit length field (LEN) of the optional data field. If data field is not present, LEN=0.

If LEN =0:

Offset 6 & 7: 16-bit checksum: MSB, then LSB. This is a two's-complement of the 16-bit sum of all bytes prior to the checksum. (i.e. the 16-bit sum of the checksum and all other bytes in the packet is 0.)

If LEN > 0:

Offset 6: The start of the data field, whose length is given by the 16-bit LEN field. The last byte is offset 5+LEN.

Offset 6+LEN, 7+LEN: Checksum, as described above.

4.1 Request Packets (Host PC to DP5)

Table 1 – Text highlighted in Blue is new/modified since Rev A6 of the Programmer's Guide

Description	Support*	PID1	PID2	LEN MSB	LEN LSB	Data (optional)	Response
Request status packet	ALL	1	1	0	0		Data packet
Request spectrum	ALL	2	1	0	0		Data packet
Request & clear spectrum	ALL	2	2	0	0		Data packet
Request spectrum + status	ALL	2	3	0	0		Data packet
Request & clear spectrum + status	ALL	2	4	0	0		Data packet
Buffer spectrum	6.08.00	2	5	0	2	Buffer # (MSB first)	ACK packet
Buffer & clear spectrum	6.08.00	2	6	0	2	Buffer # (MSB first)	ACK packet
Request buffer	6.08.00	2	7	0	2	Buffer # (MSB first)	Data packet
Request digital scope data	ALL	3	1	0	0		Data packet
Request 512-byte misc data	ALL	3	2	0	0		Data packet
Request digital scope data & re-arm scope	ALL	3	3	0	0		Data packet
Request Ethernet settings	ALL	3	4	0	0		Data packet
Request diagnostic data	ALL	3	5	0	0		Data packet
Request Netfinder packet	6.01	3	7	0	0		Data packet
Perform I2C transfer	6.01	3	8	varies		I2C transfer description	ACK or Data
Request List-mode data	6.06.05	3	9	0	0		ACK or Data
Request Option PA calibration data	6.07.02; M	3	0x0A	0	0		ACK or Data
Request 32-bit SCA counters	ALL	4	1	0	0		Data packet
Latch + Request 32-bit SCA counters	ALL	4	2	0	0		Data packet
Latch + Clear + Request 32-bit SCA counters	ALL	4	3	0	0		Data packet
Text configuration (to DP5)	ALL	0x20	2	varies		ASCII configuration	ACK packet
Text configuration Readback (from DP5)	6.01	0x20	3	varies		ASCII configuration	Data packet
Text configuration (to DP5) without saving to nonvolatile memory	6.08.00; ALL	0x20	4	varies		ASCII configuration	ACK packet
Erase FPGA image	ALL	0x30	1	0	2	0x12 0x34	ACK packet
Upload packet (FPGA)	ALL	0x30	2	varies			ACK packet
Reinitialize FPGA	6.06.01	0x30	3	0	0		
Erase uC image #1	ALL	0x30	5	0	2	0x12 0x34	ACK packet
Upload packet (uC)	ALL	0x30	7	varies			ACK packet
Switch to uC image #1	ALL	0x30	9	0	4	0xA5 0xF1 CS	ACK packet

						MSB, LSB	
Upload packet (FPGA), FPGA ACK	6.06.04	0x30	0x0B	varies			FPGA ACK packet
Clear Spectrum Buffer	ALL	0xF0	0x01	0	0		ACK packet
Enable MCA/MCS	ALL	0xF0	0x02	0	0		ACK packet
Disable MCA/MCS	ALL	0xF0	0x03	0	0		ACK packet
Arm digital oscilloscope	ALL	0xF0	0x04	0	0		ACK packet
Autoset input offset	ALL; D, P	0xF0	0x05	0	0		ACK packet
Autoset fast threshold	ALL	0xF0	0x06	0	0		ACK packet
Read IO3-0		0xF0	0x07	0	0		
Write IO3-0	ALL	0xF0	0x08	0	1		ACK packet
Write 512-byte Misc Data	ALL	0xF0	0x09	2	0		ACK packet
Set DCAL	ALL; D, P	0xF0	0x0A	0	2	LSB, MSB	ACK packet
Set PZ correction	ALL	0xF0	0x0B	0	1	PZ correction	ACK packet
Set uC temp cal	ALL	0xF0	0x0C	0	1	uC temp offset	ACK packet
Set ADC Cal (gain/offset)	ALL	0xF0	0x0E	0	2	gain, offset	ACK packet
Clear G.P. Counter	ALL	0xF0	0x10	0	0		ACK packet
Set Ethernet settings	ALL	0xF0	0x11	0	0x13	Fixed/Dyn, IP[4], Mask[4], Gateway[4], Dest. IP[4], Port[2]	ACK packet
Select high-pass time constant	6.01	0xF0	0x12	0	1	Time constant	ACK packet
Select RS232 baud rate	6.05	0xF0	0x13	0	1	Baud rate	ACK packet
Set HV Cal (gain/offset)	6.05; D, P	0xF0	0x14	0	2	gain, offset	ACK packet
Set 1.6uS PZ correction	6.06; P	0xF0	0x15	0	1	PZ correction	ACK packet
Clear/Sync List-mode timer	6.06.05	0xF0	0x16	0	0		ACK packet
Set zero offset, 1V scale	6.06.07; M	0xF0	0x19	0	2	Signed, MSB first	ACK packet
Set zero offset, 10V scale	6.06.07; M	0xF0	0x1A	0	2	Signed, MSB first	ACK packet
Restart sequential buffering	6.08.00	0xF0	0x1E	0	0		ACK packet
Cancel sequential buffering	6.08.00	0xF0	0x1F	0	0		ACK packet
Interface keep-alive - allow sharing	ALL	0xF0	0x20	0	0		ACK packet
Interface keep-alive - no sharing	ALL	0xF0	0x21	0	0		ACK packet
Interface keep-alive - lock	ALL	0xF0	0x22	0	0		ACK packet
Latch SCAs							
Latch + clear SCAs							
Clear SCAs							
Comm test - Request ACK packet	ALL	0xF1	0…15	0	0		ACK packet

Comm test - Streaming test mode	6.07.04	0xF1	0x7E	0	0 or 8	MINA MSB, LSB; MAXA MSB, LSB; INCR MSB, LSB; PERIOD MSB, LSB	ACK packet
Comm test - Echo packet	ALL	0xF1	0x7F	varies		Data to be echoed	Data packet

Items in italics are considered calibration values and don't normally need to be changed

* Initial firmware release which supports this packet type;
If not support by all three DPP types, then:
D = supported by DP5,
P = supported by PX5, and
G = supported by DP5G

4.1.1 Request packet: "Request Status Packet"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**1**	**1**	**0**	**0**	**0xFE**	**0x0F**

Purpose: This request directs the DP5 to construct a status packet and send it to the host PC. The status packet can be requested with this request packet, or with one of the 'Request Spectrum plus Status' variants, in which case the status packet is included in the packet data field along with the spectrum data.

The status packet contains information about the current state of the spectrum, and of the DP5. Its format is listed with the "Status Packet" Response Packet.

Response: If no errors are detected, a "Status Packet" Response Packet will be returned.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data.

4.1.2 Spectrum Request Packets

Request packet: "Request Spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**2**	**1**	**0**	**0**	**0xFE**	**0x0E**

Request packet: "Request and clear Spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**2**	**2**	**0**	**0**	**0xFE**	**0x0D**

Request packet: "Request Spectrum plus Status"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**2**	**3**	**0**	**0**	**0xFE**	**0x0C**

Request packet: "Request and clear Spectrum plus Status"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**2**	**4**	**0**	**0**	**0xFE**	**0x0B**

Purpose: These requests direct the DP5 to take a 'snapshot' of the spectrum and corresponding status data and begin transmitting that data. If the 'Request and Clear' form of this packet is send, it will also clear the spectrum and associated status data, and if the MCA was enabled when this request was received, then a new acquisition will start.
Response: If no errors are detected, than either a 'spectrum' response packet, or a 'spectrum plus status' response packet will be sent by the DP5.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data. If the FPGA failed initialization, then an FPGA error ACK packet will be returned. For FW6.08.00 (and later), if Sequential Buffering is active, a BUSY ACK packet is returned. (See section 6.3.)

4.1.3 Request packet: "Buffer spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-7	8	9
Value	**0xF5**	**0xFA**	**0x02**	**0x05**	**0**	**2**	**Buffer number MSB, LSB**	**varies**	

4.1.4 Request packet: "Buffer & clear spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-7	8	9
Value	**0xF5**	**0xFA**	**0x02**	**0x06**	**0**	**2**	**Buffer number MSB, LSB**	**varies**	

Purpose: These commands are similar to the 'Request Spectrum' request packets, except rather than transmitting the data immediately, these commands cause the spectrum (plus associated status data) to be buffered in onboard memory for later retrieval. The 'Buffer number' specifies which buffer slot to use – the range of buffer numbers depends on the number of MCA channels selected:

Number of Channels	Buffer number range
256	0-511
512	0-255
1024	0-127
2048	0-63
4096	0-31
8192	0-15

Support: This request is supported in FW6.08.00 and later. **See section 6.3 for more information**.

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK. If the Buffer number is outside the acceptable range, a 'Parameter error' ACK packet will be returned.

4.1.5 Request packet: "Request buffer"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-7	8	9
Value	**0xF5**	**0xFA**	**0x02**	**0x07**	**0**	**2**	**Buffer number MSB, LSB**	**varies**	

Purpose: This command is similar to the 'Request spectrum plus status' request packet, except rather than returning the current spectrum and status, this command retrieves a previously buffered spectrum plus the associated status data. The 'Buffer number' specifies which buffer slot to retrieve – the range of buffer numbers depends on the number of MCA channels selected:

Number of Channels	Buffer number range
256	0-511
512	0-255
1024	0-127
2048	0-63
4096	0-31
8192	0-15

Note that the contents of the buffer slot will be sent, whether or not a spectrum has been saved to that slot. Also, if the number of channels is changed between the buffering of the spectrum and requesting the buffer, then the format of the transmitted data will be incorrect.

Support: This request is supported in FW6.08.00 and later. **See section 6.3 for more information.**

Response: If no errors are detected, the DP5 will respond with a Spectrum response packet (see sections 4.2.2 - 4.2.13.)

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK. If the Buffer number is outside the acceptable range, a 'Parameter error' ACK packet will be returned instead of the Spectrum response packet.

4.1.6 Request packet: "Request Digital Scope Data"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**3**	**1**	**0**	**0**	**0xFE**	**0x0D**

4.1.7 Request packet: "Request Digital Scope Data & Re-arm Scope"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**3**	**3**	**0**	**0**	**0xFE**	**0x0B**

Purpose: These request that the DP5 send a 2048-byte digital scope packet. The second form of the command will also re-arm the digital scope.

Response: If no errors are detected, the DP5 will respond with a '2048-byte Scope Packet' Response Packet (PID1=0x82, PID2=1) or a '2048-byte Scope Packet w/ Overflow' Response Packet (PID1=0x82, PID2=3). (See the Response Packet descriptions for details.)

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data. Also, if no data is available because the scope hasn't triggered, a "Scope data not available" ACK packet will be returned instead of the requested data.

4.1.8 Request packet: "Request Misc Data"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**3**	**2**	**0**	**0**	**0xFE**	**0x0C**

Purpose: This requests that the DP5 send the 512-bytes of 'miscellaneous data' that is stored in the DP5's non-volatile memory. (See also the "Write Misc Data" Request Packet for information on to write this data to the DP5.)

Response: If no errors are detected, the DP5 will respond with the "512-byte Misc Data" Response Packet (PID1=0x82, PID2=2).

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data.

4.1.9 Request packet: "Request Ethernet Settings"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**3**	**4**	**0**	**0**	**0xFE**	**0x0A**

Purpose: This requests that the DP5 send the Ethernet settings that are stored in the DP5's non-volatile memory. (See also the "Set Ethernet Settings" Request Packet for information on how to write these settings.)

Response: If no errors are detected, the DP5 will respond with the "Ethernet Settings" Response Packet (PID1=0x82, PID2=4).

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data. Additionally, if no Ethernet controller is detected on the DP5, the "CP2201 not found" ACK packet will be returned instead of the requested data.

4.1.10 Request packet: "Request Diagnostic Data"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**3**	**5**	**0**	**0**	**0xFE**	**0x09**

Purpose: This requests that the DP5 perform some diagnostic tests, and return a suite of diagnostic data.

Response: If no errors are detected, the DP5 will respond with the "Diagnostic Data" Response Packet (PID1=0x82, PID2=5). Note: the DP5 runs a full memory test on the 512KB SRAM, which takes some time. The DP5 will respond with the Response Packet a maximum of 2.5s after receiving the Request Packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data.

4.1.11 Request packet: "Request Netfinder Packet"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**3**	**7**	**0**	**0**	**0xFE**	**0x07**

Purpose: This requests a Netfinder packet, but through the active communications port. [The 'Netfinder packet' is generally obtained via a broadcast on the TCP/IP Netfinder socket. See section 3.2.4 for details.]

Response: If no errors are detected, the DP5 will respond with the "Netfinder Packet" Response Packet (PID1=0x82, PID2=8).

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data.

4.1.12 Request packet: "I²C Transfer"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6…5+LEN	6+LEN	7+LEN
Value	**0xF5**	**0xFA**	**3**	**8**	**varies**		**varies**	**varies**	

Purpose: The data field of this Request Packet contains the description for an I²C transfer to be performed by the DP5. Read, Write and Combined I²C transfers are supported.

The format of the data field is listed below. The first 3 bytes are mandatory; following those are the bytes to be written, which can number from 0 to a maximum of 32. Therefore, the size of the data field (LEN) has a minimum of 3 and a maximum of 35.

Data Offset	Allowed Values	Value
0	1-127	7-bit I²C slave address ('SA')
1	0-32	Number of bytes to read ('NOBR')
2	0-32	Number of bytes to write ('NOBW')
3-34	0-255	Bytes to be written (optional)

Note: The DP5 uses Slave Addresses of 0x20 and 0x4C. The optional PC5 uses Slave Addresses of 0x1F, 0x34, 0x50 and 0x6D. Transfers should not be attempted using these Slave Addresses. Also, the value in offset 0 is the 7-bit address – this value will be shifted left one bit, and the appropriate R/W bit merged in, before it's transmitted on the I²C bus.

Response: If no errors are detected, the DP5 will respond either with an ACK OK packet (if NOBR=0), or with an I²C Response Packet with the bytes read from the I²C slave (if NOBR > 0).

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data or the ACK OK packet. If the I²C master didn't detect the I²C ACK at the proper time, an 'I²C ERROR' ACK packet will be returned. A BAD PARAMETER ACK packet will be returned if there are structure problems with the request. (NOBR=NOBW=0; LEN not equal to NOBW+3; NOBR > 32; NOBW > 32; or SA = 0).

4.1.13 Request packet: "Request List-Mode Data"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**3**	**9**	**0**	**0**	**0xFE**	**0x05**

Purpose: This requests that the DP5 send available List-mode data.

Response: A 'List-mode data' Response Packet (PID1=0x82, PID2=9) will be returned, with between 0 and 1020 records (0 to 4092 bytes.) If the List-mode FIFO is full, a 'List-mode data, FIFO full' Response packet (PID1=0x82, PID2=10) is returned, which will contain 1024 records. [The FIFO size may be increased in future FPGA versions; hence, the two different response packets, rather than having the application monitor the returned data size.]

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data. Additionally, if the firmware has been upgraded for List-mode support, but the FPGA hasn't, a 'Feature not supported by this FPGA version' ACK packet will be returned instead of the List-mode data Response Packet.

Note: The 'Clear Spectrum' Request Packet clears the List-mode FIFO, in addition to clearing the spectrum buffer.

4.1.14 Request packet: "Request Option PA calibration data" [MCA8000D only]

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**3**	**0x0A**	**0**	**0**	**0xFE**	**0x04**

Purpose: This requests the MCA8000D Option PA calibration data, if available.

Response: If the MCA8000D has the Option PA calibration installed, then an Option PA Calibration Data Response Packet will be returned.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data. Additionally, if the Option PA calibration has not been performed on this MCA8000D, a 'Calibration data not present' ACK packet will be returned instead of the Option PA Calibration Data Response Packet.

4.1.15 Request packet: "Request 32-bit SCA Counters"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**4**	**1**	**0**	**0**	**0xFE**	**0x0C**

4.1.16 Request packet: "Latch + Request 32-bit SCA Counters"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**4**	**2**	**0**	**0**	**0xFE**	**0x0B**

4.1.17 Request packet: "Latch + Clear + Request 32-bit SCA Counters"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**4**	**3**	**0**	**0**	**0xFE**	**0x0A**

Purpose: These request that the DP5 send 64 bytes of SCA counter data (16 SCAs x 32 bits each). The data is read from the SCA counter latches, so the SCAs must have been latched, either via the 'Latch' form of these requests, a 'Latch SCA' Request Packet (which is TBD in FW6.01), or a hardware signal (also TBD.) The 'Clear' form of these requests will clear the SCA counters after the data has been latched.

Response: If no errors are detected, the DP5 will respond with a "64-byte SCA Packet" Response Packet (PID1=0x83, PID2=1).

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data.

4.1.18 Request packet: "Text Configuration"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6…5+LEN	6+LEN	7+LEN
Value	**0xF5**	**0xFA**	**0x20**	**2**	**varies**		**varies**	**varies**	

Purpose: This sends a Text Configuration packet to the DP5, which the DP5 interprets and executes. (See the section on ASCII Commands for information on individual commands.) The commands are packed into the Data field, with the following rules:

1. Alphabetic characters must be uppercase.
2. Each command consists of a 4-character command, followed by "=", followed by the parameter (max of 10 characters), and terminated by a semicolon (Ex: "TPEA=10;")
3. Units may be included with the parameter, but they are ignored, and count towards the 10-character maximum length for the parameter. (Ex: "TPEA=10US;")
4. The commands are packed together with no whitespace of any kind (tabs, spaces, CR/LF, etc.)
5. **For some commands, the ordering is important**. See the 'ASCII Commands' section for more discussion of this.
6. If all commands fit in the max 512 byte data field, then the configuration can be sent as a single packet. If they don't fit, then additional Text Configuration packets can be sent. Generally, the ASCII Command "RESC=Y;" would be the first command of the first packet, and it would not appear in later packets. If additional packets are needed, ensure that commands are not chopped between packets – only complete command/parameter strings are allowed.

   Here's an example of the data field:
   RESC=YES;CLCK=AUTO;TPEA=10US;TFLA=0US;CUSP=50%;
   RESL=3000US;PDMD=NORM;THSL=1.00%;THFA=40;

Note: After the corresponding ACK Packet is sent, the configuration is written into Flash memory. This process takes anywhere from 80-400mS, during which time further packet processing is stalled. So, if a Request Packet is received immediately after the Text Configuration Request Packet is acknowledged, the corresponding ACK packet may be delayed by up to 400mS.

Response: If no errors are detected, the DP5 will respond with an ACK OK packet. This indicates that all commands were recognized and executed without error.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data. If one or more errors are detected while parsing the Text Configuration, an 'Unknown/Bad Parameter', 'Unrecognized Command', or 'PC5 Not Present' ACK packet will be returned, and the data field will contain the ASCII command and parameter which caused the error. If more than one error was detected, only the last error & command will be returned.

4.1.19 Request packet: "Text Configuration Readback"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6…5+LEN	6+LEN	7+LEN
Value	**0xF5**	**0xFA**	**0x20**	**3**	**varies**		**varies**	**varies**	

Purpose: This sends a Text Configuration Readback Request Packet to the DP5, which the DP5 uses as a 'template' to read back the current configuration. The data field is the same format as for the Text Configuration Request Packet – a list of ASCII command and parameters, separated by semicolons. The DP5 strips off any parameters and replaces them with the current settings for each command specified. The result is returned in the Configuration Readback Response Packet. It is possible to send a text configuration packet via the Text Configuration Request Packet (PID1=0x30 / PID2=2), and then reuse the same packet data field for the Text Configuration Readback Request Packet (PID1=0x30 / PID2=3) to read back the actual settings that the DP5 derived from the Text Configuration packet.

The "=" and parameter are optional for each command listed; the minimum required is the 4-character commands, separated by semicolons. There is one exception to this – the SCAI (SCA Index) command. As this is a directive to the command processor rather than a true command, the '=' and parameter are required. Here is an example data field, to read back the low and high thresholds for SCA1 & SCA2: "SCAI=1;SCAL;SCAH;SCAI=2;SCAL;SCAH;"

Also note that the 'RESC' (Reset Configuration) has no meaning in the context of Configuration Readback – if included, it will return 'RESC=?;'.

Any number of commands may be read back, as long as they fit within the maximum data field of 512 bytes. As of FW6.01, there is no error handling for the condition where the generated Response Packet exceeds the maximum data field size, so limiting the size of the Request Packet data field is a good idea, to avoid this issue.

Response: If no errors are detected, the DP5 will respond with a Configuration Readback Response Packet (PID1=0x82 / PID2 = 7). Any command which is not recognized in the data field will return "CMDA=??;", where 'CMDA' is the unknown command. [This is returned in the Response Packet with the rest of the commands.]

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data. If one or more errors are detected while parsing the Text Configuration, an 'Unknown/Bad Parameter', 'Unrecognized Command', or 'PC5 Not Present' ACK packet will be returned, and the data field will contain the ASCII command and parameter which caused the error. If more than one error was detected, only the last error & command will be returned.

4.1.20 Request packet: "Text Configuration (without saving to nonvolatile memory)"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6…5+LEN	6+LEN	7+LEN
Value	**0xF5**	**0xFA**	**0x20**	**4**	**varies**		**varies**	**varies**	

Purpose: This packet is identical to the 'Text Configuration' Request Packet (PID1/PID2=0x20/0x02), with one exception: the received configuration data is not written to non-volatile memory, so this configuration will not be the default when the device is next powered on.

Under certain circumstances, the delay in writing the data to Flash memory can be an issue, so this Request Packet allows that issue to be avoided. Section 4.1.18 discusses this in more detail.

Support: This request is supported in FW6.08.00 and later.

Response: If no errors are detected, the DP5 will respond with an ACK OK packet. This indicates that all commands were recognized and executed without error.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested data. If one or more errors are detected while parsing the Text Configuration, an 'Unknown/Bad Parameter', 'Unrecognized Command', or 'PC5 Not Present' ACK packet will be returned, and the data field will contain the ASCII command and parameter which caused the error. If more than one error was detected, only the last error & command will be returned.

4.1.21 Request packet: "Clear Spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**1**	**0**	**0**	**0xFD**	**0x20**

Purpose: This commands the DP5 to clear the MCA (spectrum), and all associated values (see section 4.2.1 for a list of what fields in the status packet are cleared by this command.)
. If the acquisition was enabled when this command was received, it will continue to be enabled after the spectrum is cleared. It also resets the List-mode FIFO to empty.

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.22 Request packet: "Enable MCA/MCS"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**2**	**0**	**0**	**0xFD**	**0x1F**

Purpose: This commands the DP5 to enable the MCA. If the acquisition was stopped due to a "Disable MCA/MCS" command or because the 'Preset Time' expired, this command will re-enable the acquisition, without clearing anything. If the acquisition was stopped due to 'Preset Counts' being reached, then this command will have no effect until the spectrum is cleared. (See ASCII Commands PREC & PRET.)

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.23 Request packet: "Disable MCA/MCS"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**3**	**0**	**0**	**0xFD**	**0x1E**

Purpose: This commands the DP5 to disable the MCA, effectively pausing the acquisition.

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.24 Request packet: "Arm Digital Scope"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**4**	**0**	**0**	**0xFD**	**0x1D**

Purpose: This commands the DP5 to arm its internal digital oscilloscope. Once armed, a trigger condition will cause the digital scope to capture 2048 samples. After arming the digital scope, the application software can either:

1. Monitor the 'Oscilloscope data ready' bit (offset 35: bit D2 in the status data) to determine when the scope has triggered, then send a "Request Digital Scope Data" request packet to get the data.
2. Repeatedly send a "Request Digital Scope Data" request packet – the DP5 will respond with a "Scope data not available" ACK packet if the trigger hasn't occurred yet. It will respond with the "2048-byte scope packet" or "2048-byte scope packet w/ overflow" after the scope has triggered.

   (See the DACO, SCOE, SCOT & SCOG ASCII commands for more information on the Digital Scope.)

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.25 Request packet: "Autoset Input Offset"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**5**	**0**	**0**	**0xFD**	**0x1C**

Purpose: This commands the DP5 to search for an appropriate input offset (i.e. the DC offset of the input signal as seen by the input ADC.) Generally, the 'default' input offset should work with most detectors. (See the INOF ASCII command.) In order for the Autoset Input Offset function to work properly:

1. The input polarity must be set properly (see the AINP ASCII command.)
2. HV & detector temperature (if applicable) must be reasonably stable.
3. An appropriate input offset might not be found if this command is initiated while the input count rate is high.

Support: This request is supported by the DP5 and PX5, but not the DP5G. (The DP5G does not have a variable input offset.)

Response: If no errors are detected, the DP5 will respond with ACK OK packet. The DP5 sends the ACK packet immediately, and does not wait for the Autoset function to complete. The result of this command is in the status data (offset 36: bit D7) – it returns "Auto Input Offset locked" or "Auto Input Offset searching". Status can be polled until the result indicates 'locked'.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.26 Request packet: "Autoset Fast Threshold"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**6**	**0**	**0**	**0xFD**	**0x1B**

Purpose: This commands the DP5 to search for an appropriate fast threshold setting. In order for the Autoset Fast Threshold function to work properly, no input counts can be present (other than noise.)

Response: If no errors are detected, the DP5 will respond with ACK OK packet. The DP5 sends the ACK packet immediately, and does not wait for the Autoset function to complete. The result of this command is in the status data (offset 35: bit D6) – it returns "Auto Fast Threshold not locked" or "Auto Fast Threshold locked". Status can be polled until the result indicates 'locked'. The fast threshold determined by this function is returned by the readback of the 'THFA' command, using the 'Text Configuration Readback' Request Packet. Note that this setting is overwritten when a new configuration packet is received with the "THFA" or "RESC" commands.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.27 Request packet: "Write IO3-0"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7	8
Value	**0xF5**	**0xFA**	**0xF0**	**8**	**0**	**1**	**IO3…IO0**	**varies**	

Purpose: This commands the DP5 to set the four IO lines IO3-0 with the data byte in offset 6, as shown below. Note that these outputs are open-drain, with a weak pullup. They can sink 20mA, but only source 100uA (typ) at 3.3V. (These are outputs from a Maxim MAX7328 operating at 3.3V – see the datasheet for more info.)

Bit	Signal	DP5 Connector Location	PX5 Connector Location
D7-D4	-	N/A	N/A
D3	IO3	J6.14 (Auxiliary connector)	J5.10 (internal header)
D2	IO2	J6.13 (Auxiliary connector)	J5.9 (internal header)
D1	IO1	J5.18 (Interconnect connector)	J5.8 (internal header)
D0	IO0	J5.17 (Interconnect connector)	J5.7 (internal header)

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.28 Request packet: "Write 512-byte Misc Data"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-517	518	519
Value	**0xF5**	**0xFA**	**0xF0**	**9**	**2**	**0**	**Misc Data**	**varies**	

Purpose: This commands the DP5 to store the 512-byte data field in non-volatile memory. The data can be binary, ASCII, etc. (It could contain the description or location of the unit as an ASCII string, for example.) It is read back with the "Request Misc Data" Request Packet.

Response: If no errors are detected, the DP5 will respond with ACK OK packet. Note this command requires a FLASH memory erase operation – the ACK packet could be delayed as much as 400mS from the request packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.29 Request packet: "Set DCAL"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-7	8	9
Value	**0xF5**	**0xFA**	**0xF0**	**0x0A**	**0**	**2**	**DCAL LSB, MSB**	**varies**	

Purpose: This commands the DP5 to set the non-volatile calibration value for the detector temperature measurement diode. The setting is an unsigned integer in the range of 0-4095, in the format LSB followed by MSB. The nominal value is 1.000V, which corresponds to a setting of 0x555. (The conversion factor is 732uV/count.) This value can be read back via the "Request Diagnostic Packet" Request Packet. The setting is stored in the DP5 non-volatile memory. If a PC5 is present, it is also stored in the PC5 non-volatile memory.

Support: This request is supported by the DP5 and PX5, but not the DP5G.

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.30 Request packet: "Set PZ Correction"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7	8
Value	**0xF5**	**0xFA**	**0xF0**	**0x0B**	**0**	**1**	**PZ Corr**	**varies**	

Purpose: This commands the DP5 to set the non-volatile correction factor for the Pole-Zero. This allows digital fine-tuning of the analog PZ time constant. (This calibration value is set at the factory and shouldn't need to be changed.) This value can be read back via the "Request Diagnostic Packet" Request Packet. The interpretation of the PZ Correction value ('setting') is:

Setting of 0-127: the correction factor is (1024+setting)/1024 (i.e. 100% to 112.4%)
Setting of 128-255: the correction factor is (768+setting)/1024 (i.e. 87.5% to 99.9%)
Examples: setting = 0 -> 100% correction factor;
setting =10 -> 101% correction factor;
setting =250-> 99.4% correction factor

The PX5 has two software-selectable pole-zero filters. This command sets the calibration for the 3.2uS pole-zero. The DP5 and DP5G have a single pole-zero; this command sets the calibration for it.

Note: This command won't take effect until the next configuration request packet is received.

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.31 Request packet: "Set uC Temperature Calibration"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7	8
Value	**0xF5**	**0xFA**	**0xF0**	**0x0C**	**0**	**1**	**uC Temp Cal**	**varies**	

Purpose: This commands the DP5 to set the non-volatile offset calibration for the DP5 temperature measurement. It is an 8-bit signed value, and is added to the measured temperature; the result appears in the status data as 'board temperature' (offset 34). This value can be read back via the "Request Diagnostic Packet" Request Packet. [The temperature sensor is internal to the microcontroller; this calibration value allows compensation for the fact that the uC die is always hotter than the board.]

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.32 Request packet: "Set ADC Calibration"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-7	8	9
Value	**0xF5**	**0xFA**	**0xF0**	**0x0E**	**0**	**2**	**Gain, Offset**	**varies**	

Purpose: This commands the DP5 to set the non-volatile gain and offset calibration values for the DP5 ADC. These values can be read back via the "Request Diagnostic Packet" Request Packet.

Gain: If gain setting is 0-127: Correction = (1024+setting)/1024 (i.e. 100% to 112.4%)
If gain setting is 128-255: Correction = (768+setting)/1024 (i.e. 87.5% to 99.9%)
Offset: The offset setting is a signed byte.
Calibrated ADC Value = (Raw ADC Value * Gain) + Offset.

Note: This command won't take effect until the next configuration request packet is received.

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.33 Request packet: "Clear G.P. Counter"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**0x10**	**0**	**0**	**0xFD**	**0x11**

Purpose: This commands the DP5 to clear the General Purpose Counter ("G.P. Counter"). (See the ASCII commands GPIN, GPED, GPME, GPGA and GPMC for more information on the G.P. Counter.)

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.34 Request packet: "Set Ethernet Settings"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-24	25	26
Value	**0xF5**	**0xFA**	**0xF0**	**0x11**	**0**	**0x13**	**Ethernet settings**	**varies**	

Purpose: This commands the DP5 to set the IP address, etc. for the Ethernet controller. The current values can be read back via the "Request Ethernet Settings" Request Packet.

The format of the data field is:

Data Offset	Value
0	0 = Use fixed IP address; 0xFF = Get IP address from DHCP server
1-4	IP Address (MSB…LSB)
5-8	IP Subnet Mask (MSB…LSB)
9-12	IP Gateway Address (MSB…LSB)
13-16	Reserved
17-18	Port (MSB,LSB: fixed at 10001 for FW6.01)

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK. Additionally, if no Ethernet controller is detected on the DP5, the "CP2201 not found" ACK packet will be returned instead of ACK OK.

4.1.35 Request packet: "Select High-Pass Time Constant"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7	8
Value	**0xF5**	**0xFA**	**0xF0**	**0x12**	**0**	**1**	**Time Constant**	**varies**	

Purpose: This selects which high-pass time constant the DP5's front end is set for. (The time constant is determined by what resistor values are installed – this Request Packet is used to configure the firmware appropriately. The setting is saved in non-volatile memory, so this Request Packet only needs to be sent if the time constant is changed.) This value can be read back via the "Request Diagnostic Packet" Request Packet. The interpretation of the high-pass time constant value ('setting') is:

0 => 1.625uS time-constant;
1 => 3.225uS time-constant;
2 => 6.425uS time-constant;
3 => 12.825uS time-constant;
4 => 25.625uS time-constant

The PX5 has two selectable poles – 1.625uS and 3.225uS. This command will switch the appropriate pole into the front end. If >3.225uS is selected, then the PX5 will select the 3.2uS slot – component changes are required to convert that slot to the selected time constant. Contact Amptek for more information.

Note: This command won't take effect until the next configuration request packet is received.

Response: If no errors are detected, the DP5 will respond with ACK OK packet. If the data byte is outside the range of 0-5, then a BAD PARAMETER error is returned.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.36 Request packet: "Select RS232 Baud Rate"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7	8
Value	**0xF5**	**0xFA**	**0xF0**	**0x13**	**0**	**1**	**Baud Rate**	**varies**	

Purpose: This selects the RS232 baud rate. The default is 115,200 baud. 57,600 baud or 19,200 baud can be selected; however, these setting are incompatible with the Ethernet stack. Therefore, **selecting 57,600 baud or 19,200 baud will disable the Ethernet interface**. When this value is changed, the new setting will not take effect until the next power cycle. The interpretation of the baud rate value ('setting') is:

0 => 115,200 baud;
1 => 57,600 baud;
2 => 19,200 baud;

Response: If no errors are detected, the DP5 will respond with ACK OK packet. If the data byte is outside the range of 0-2, then a BAD PARAMETER error is returned.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.37 Request packet: "Set HV Calibration"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-7	8	9
Value	**0xF5**	**0xFA**	**0xF0**	**0x14**	**0**	**2**	**Gain, Offset**	**varies**	

Purpose: This commands the DP5 [PX5] to set the non-volatile gain and offset calibration values for the PC5 [PX5] HV DAC. These values can be read back via the "Request Diagnostic Packet" Request Packet.

Gain: If gain setting is 0-127: Correction = (1024+setting)/1024 (i.e. 100% to 112.4%)
If gain setting is 128-255: Correction = (768+setting)/1024 (i.e. 87.5% to 99.9%)
Offset: The offset setting is a signed byte, with a scale factor of 366mV/LSB.
Calibrated DAC Value = (Raw DAC Value * Gain) + Offset.

Response: If no errors are detected, the DP5 [PX5] will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.38 Request packet: "Set 1.6uS PZ Correction" [PX5 only]

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7	8
Value	**0xF5**	**0xFA**	**0xF0**	**0x15**	**0**	**1**	**PZ Corr**	**varies**	

Purpose: The PX5 has two software selectable pole-zero settings; 1.6uS and 3.2uS. This commands the PX5 to set the non-volatile correction factor for the 1.6uS Pole-Zero. This allows digital fine-tuning of the analog PZ time constant. (This calibration value is set at the factory and shouldn't need to be changed.) This value can be read back via the "Request Diagnostic Packet" Request Packet. The interpretation of the PZ Correction value ('setting') is:

Setting of 0-127: the correction factor is (1024+setting)/1024 (i.e. 100% to 112.4%)
Setting of 128-255: the correction factor is (768+setting)/1024 (i.e. 87.5% to 99.9%)
Examples: setting = 0 -> 100% correction factor;
setting =10 -> 101% correction factor;
setting =250-> 99.4% correction factor

Note: This command won't take effect until the next configuration request packet is received.

Response: If no errors are detected, the PX5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.39 Request packet: "Clear/Sync List-mode timer"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**0x16**	**0**	**0**	**0xFD**	**0x0B**

Purpose: This request packet sets the List-mode timer to zero, and will cause a time-tag event to be written to the List-mode FIFO.

Response: If no errors are detected, the device will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.40 Request packet: "Restart Sequential Buffering"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**0x1E**	**0**	**0**	**0xFD**	**0x03**

Purpose: This request packet starts (or restarts) the Sequential buffering mode of operation. **(See section 6.3 for detailed information on this mode, including timing information).** This mode uses a hardware strobe to trigger the buffering of spectrum plus associated status data. This command resets the buffer pointer to buffer slot 0, so that in response to the next hardware trigger, buffer slot 0 will be used. The number of buffer slots is dependent on the number of channels currently configured as follows:

Number of Channels	Number of buffer slots
256	512
512	256
1024	128
2048	64
4096	32
8192	16

The "AUX_IN2" signal is used as the hardware strobe. The buffering is triggered by the rising edge of this signal. (For the PX5 and DP5G, use the 'CON2' ASCII command to connect the AUX_IN2 signal for the AUX-2 connector.) The period of the strobe needs to be greater than the buffering time (listed in section 3.4 as buffering 'deadtime'), and the minimum pulse width is 400 nS. (See section 6.3 for detailed information).

After receipt of this command, Sequential Buffering will continue to buffer spectra in response to the hardware signal until all buffers are full, or until the 'Cancel sequential buffering' command is received.

Response: If no errors are detected, the device will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.41 Request packet: "Cancel Sequential Buffering"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**0x1E**	**0**	**0**	**0xFD**	**0x03**

Purpose: This request packet cancels the Sequential buffering mode of operation. (See section 6.3 for detailed information on this mode). After receipt of this command, the hardware strobe will no longer cause buffering of spectra.

After receipt of this command, Sequential Buffering will continue to buffer spectra in response to the hardware signal until all buffers are full, or until the 'Cancel sequential buffering' command is received.

Response: If no errors are detected, the device will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.42 Request packet: "Interface Keep-alive – Allow Sharing"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**0x20**	**0**	**0**	**0xFD**	**0x01**

Purpose: This Request Packet is used to keep the DP5's UDP socket bound to the IP address and source port of the computer connected to it. The UDP socket resets itself after 15 seconds of inactivity (after which any IP address can connect to it), so one of the "Interface Keep-alive" Request Packets should be sent periodically if there is no other periodic traffic, or if the periodic traffic is less frequent than ~10 seconds. [If the host wishes to change the Keep-alive status (sharing/no sharing/locked), then a Keep-alive packet should be sent with the new status, even if there is periodic traffic keeping the socket bound.]

The "Allow Sharing" variant of the "Interface Keep-alive" Request Packet tells the DP5 to return the "Sharing Allowed" status in the Netfinder device discovery packet. It also commands the DP5 to accept "Interface Sharing Request" packets on the Netfinder socket, and to return an "Ethernet Sharing Request" ACK packet via the normal UDP socket if such a packet is received. [This ACK packet will replace an OK ACK packet at the next opportunity.]

[As of FW6.01, this Request Packet only applies to Ethernet. In future firmware, it may be expanded to include the other interfaces.]

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.43 Request packet: "Interface Keep-alive – No Sharing"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**0x21**	**0**	**0**	**0xFD**	**0x00**

Purpose: This Request Packet is used to keep the DP5's UDP socket bound to the IP address and source port of the computer connected to it. The UDP socket resets itself after 15 seconds of inactivity (after which any IP address can connect to it), so one of the "Interface Keep-alive" Request Packets should be sent periodically if there is no other periodic traffic, or if the periodic traffic is less frequent than ~10 seconds. [If the host wishes to change the Keep-alive status (sharing/no sharing/locked), then a Keep-alive packet should be sent with the new status, even if there is periodic traffic keeping the socket bound.]

The "No Sharing" variant of the "Interface Keep-alive" Request Packet tells the DP5 to return the "No Sharing" status in the Netfinder device discovery packet. It also commands the DP5 to ignore "Interface Sharing Request" packets on the Netfinder socket.

[As of FW6.01, this Request Packet only applies to Ethernet. In future firmware, it may be expanded to include the other interfaces.]

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.44 Request packet: "Interface Keep-alive – Lock"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF0**	**0x22**	**0**	**0**	**0xFC**	**0xFF**

Purpose: This Request Packet is used to keep the DP5's UDP socket bound to the IP address and source port of the computer connected to it. Normally, the UDP socket resets itself after 15 seconds of inactivity (after which any IP address can connect to it), but it will not automatically reset itself after receiving this Request Packet (so periodic transfers are no longer required to keep the socket bound.) [If the host wishes to change the Keep-alive status (sharing/no sharing/locked), then a Keep-alive packet should be sent with the new status]

The "Lock" variant of the "Interface Keep-alive" Request Packet tells the DP5 to return the "Lock" status in the Netfinder device discovery packet. It also commands the DP5 to ignore "Interface Sharing Request" packets on the Netfinder socket, and to not automatically reset the socket. Care must be taken in using this; the UDP socket binds to the IP Address and source port of the host, so the DP5 will then only communicate with the same IP & source port. The host IP address may change if the host uses a dynamic IP address; the source port may change if the host wishes to communicate with multiple DP5s simultaneously, or doesn't set the source port explicitly. If the host loses the ability to communicate with the socket, then the power will have to be cycled on the DP5 to reset the socket.

[As of FW6.01, this Request Packet only applies to Ethernet. In future firmware, it may be expanded to include the other interfaces.]

Response: If no errors are detected, the DP5 will respond with ACK OK packet.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of ACK OK.

4.1.45 Request packet: "Comm test - Request ACK packet"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	**0xF5**	**0xFA**	**0xF1**	**0..15**	**0**	**0**	**varies**	

Purpose: This Request Packet is handy for software developers – it requests that a specific ACK packet be returned in response to the request. (It's useful for testing application error handling – this is much easier than trying to force the various error conditions.) The value of PID2 is used as PID2 in the ACK packet; i.e. sending the Request Packet PID1=0xF1/**PID2=4** will yield a 'Checksum Error" ACK packet (PID1=0xFF/**PID2=4**).

Response: An ACK packet, with PID2 equal to the PID2 of the Request Packet. This allows all types of ACK packets to be returned.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the requested ACK type.

4.1.46 Request packet: "Comm test – Streaming test mode"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	DATA FIELD	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5		6	7
Value	**0xF5**	**0xFA**	**0xF1**	**0x7E**	**0**	**0**	**none**	**0xFC**	**0xA2**
Offset	0	1	2	3	4	5	6…13	14	15
Value	**0xF5**	**0xFA**	**0xF1**	**0x7E**	**0**	**8**	**MINA MSB, LSB; MAXA MSB, LSB; INCR MSB, LSB; PERIOD MSB, LSB**	**varies**	

Purpose: This Request Packet switches on an internal digital pulser, which creates a stream of predictable events. These events appear in the MCA spectrum (if enabled), List-mode data (if configured), the streaming mode port (if configured), and the SCAs (if configured appropriately). Note that this digital pulser does not stimulate the fast channel, so neither pile-up nor RTD can be simulated/tested.

There are two forms of the command:

1. A Request Packet with LEN=0 (i.e. no data field) will turn off the streaming test mode, and return to normal operation.
2. A Request Packet with LEN=8 enables the streaming test mode. There are four 16-bit parameters in the data field:
   'MINA' – the minimum 14-bit (i.e. 16K channel) amplitude, in 16K channel number;
   'MAXA' – the maximum 14-bit amplitude, in 16K channel number;
   'INCR' – amplitude increment from one event to the next;
   'PERIOD' – the number of FPGA clocks between events (1 clock = 50nS @ 20MHz; 1 clock = 12.5nS @ 80MHz). The actual period is (PERIOD+1) * 50nS (or 12.5nS). The minimum is 8.

The streaming test mode will operate continuously, starting by generating an event with amplitude MINA. After PERIOD+1 clocks, an event with amplitude MINA+INCR will be generated. This process is repeated until an event would be larger than MAXA, at which point an event with amplitude of MINA is again generated. This cycle repeats until disabled by:

1. A Streaming Test Mode Request packet with LEN=0;
2. A 'Reset Configuration' ('RESC=Y;') command is received, normally at the start of a text configuration packet;
3. Power is cycled. The Streaming test mode settings are not saved in non-volatile memory; hence, they are cleared by a power cycle.

Response: An ACK packet will be returned if there are no errors.

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the Response Packet. If LEN does not equal 0 or 8, a LEN error ACK packet is returned.

4.1.47 Request packet: "Comm test - Echo packet"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	DATA FIELD	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6…5+LEN	6+LEN	7+LEN
Value	**0xF5**	**0xFA**	**0xF1**	**0x7F**	**varies**		**Data to be echoed**	**varies**	

Purpose: This Request Packet is handy for software developers – it requests that the DP5 return a Response Packet, whose length and data field are the same as those of this Request Packet – essentially, it echoes the data field in a Response Packet.

Response: If no errors are detected, the DP5 will respond with "Comm test - Echo packet" Response Packet (PID1=0xF1/PID2=0x7F).

Possible errors: If the request packet is malformed or corrupted: CHKSUM, LEN, or PID error ACK packets can be returned instead of the Response Packet.

4.2 Response Packets

Table 2– Text highlighted in Blue is new/modified since Rev A6 of the Programmer's Guide

Description	Support*	PID1	PID2	LEN MSB	LEN LSB	Data (optional)
Status Packet	ALL	0x80	1	0	0x40	See description
256-channel Spectrum	ALL	0x81	1	0x03	0	See description
256-channel Spectrum + status	ALL	0x81	2	0x03	0x40	See description
512-channel Spectrum	ALL	0x81	3	0x06	0	See description
512-channel Spectrum + status	ALL	0x81	4	0x06	0x40	See description
1024-channel Spectrum	ALL	0x81	5	0x0C	0	See description
1024-channel Spectrum + status	ALL	0x81	6	0x0C	0x40	See description
2048-channel Spectrum	ALL	0x81	7	0x18	0	See description
2048-channel Spectrum + status	ALL	0x81	8	0x18	0x40	See description
4096-channel Spectrum	ALL	0x81	9	0x30	0	See description
4096-channel Spectrum + status	ALL	0x81	0x0A	0x30	0x40	See description
8192-channel Spectrum	ALL	0x81	0x0B	0x60	0	See description
8192-channel Spectrum + status	ALL	0x81	0x0C	0x60	0x40	See description
2048-byte scope packet	ALL	0x82	1	8	0	See description
512-byte misc data packet	ALL	0x82	2	2	0	See description
2048-byte scope packet w/ overflow	ALL	0x82	3	8	0	See description
Ethernet settings	ALL	0x82	4	0	0x17	See description
Diagnostic data	ALL	0x82	5	1	0	See description
Configuration readback packet	6.01	0x82	7	varies		
Netfinder packet	6.01	0x82	8	varies		
I^2C Read Data	6.01	0x82	9	varies		See description
List-mode data	6.06.05	0x82	0x0A	varies		See description
List-mode data, FIFO full	6.06.05	0x82	0x0B	varies		See description
MCA8000D calibration packet	6.07.02; M	0x82	0x0C	0	9	See description
64-byte SCA packet	ALL	0x83	1	0	0x40	See description
Comm test - Echo packet	ALL	0x8F	0x7F	varies		Echo data

* Initial firmware release which supports this packet type

4.2.1 Response packet: "Status Packet"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-69	70	71
Value	0xF5	0xFA	**0x80**	**1**	0	0x40	Status data	varies	

Purpose: This response packet is returned in response to a 'Request Status Packet' Request Packet.

Data Format: The data field contains 64 bytes of status data. The format is given below. (This format also applies to the 64-byte status field in the "Spectrum plus Status" Response Packets.)

Note: Values in italics are cleared or zeroed by the 'Clear Spectrum', 'Request and clear Spectrum', and 'Request and clear Spectrum plus Status' request packets.

Text highlighted in Blue is new/modified since Rev A7 of the Programmer's Guide

Offset	Data bits	Allowed value	Description	Notes
0	D7-D0	0-255	*Fast count LSB*	
1	D7-D0	0-255	*Fast count byte 2*	
2	D7-D0	0-255	*Fast count byte 3*	
3	D7-D0	0-255	*Fast count MSB*	
4	D7-D0	0-255	*Slow count LSB*	'Slow counts' are counts from the slow (shaped) channel. Any event that is counted in the spectrum is also counted here.
5	D7-D0	0-255	*Slow count byte 2*	
6	D7-D0	0-255	*Slow count byte 3*	
7	D7-D0	0-255	*Slow count MSB*	
8	D7-D0	0-255	*General Purpose Counter LSB*	The G.P. Counter can be configured to count a number of different events.
9	D7-D0	0-255	*G. P. Counter byte 2*	
10	D7-D0	0-255	*G. P. Counter byte 3*	
11	D7-D0	0-255	*G. P. Counter MSB*	
12	D7-D0	0-99	*Acc. Time (0-99, 1mS/count)*	
13	D7-D0	0-255	*Acc. Time LSB, 100mS/count*	
14	D7-D0	0-255	*Acc. Time byte 2*	
15	D7-D0	0-255	*Acc. Time MSB*	
16	D7-D0	0-255	TBD	*MCA8000D: Livetime (same encoding as Realtime, below) DP5, PX5, DPG: not used*
17	D7-D0	0-255	TBD	
18	D7-D0	0-255	TBD	
19	D7-D0	0-255	TBD	
20	D7-D0	0-255	*Realtime LSB (1mS/count)*	FW6.01 and later
21	D7-D0	0-255	*Realtime byte 2*	
22	D7-D0	0-255	*Realtime byte 3*	
23	D7-D0	0-255	*Realtime MSB*	
24	D7-D4	6-15	Firmware version, major	
	D3-D0	0-15	Firmware version, minor	
25	D7-D4	5-15	FPGA version, major	
	D3-D0	0-15	FPGA version, minor	
26	D7-D0	0-255	Serial Number LSB	
27	D7-D0	0-255	Serial Number byte 2	

28	D7-D0	0-255	Serial Number byte 3	
29	D7-D0	0-255	Serial Number MSB	
30	D7-D0	0-255	HV MSB	DP5G: N/A
31	D7-D0	0-255	HV LSB (signed integer, 0.5V/count)	
32	D7-D4	0	(unused)	
	D3-D0	0-15	Detector temperature MSB	DP5G: N/A
33	D7-D0	0-255	Detector temperature LSB (0.1 degree Kelvin/count)	
34	D7-D0	-128…+127	Board temp (1 °C/count, signed)	
35	D7	0	Preset real time not reached (or not enabled)	
		1	*Preset real time reached, MCA stopped*	
	D6	0	Auto Fast Threshold not locked	MCA8000D: 0=Preset Livetime not reached (or not enabled); 1=Preset Livetime reached, MCA stopped
		1	Auto Fast Threshold locked	
	D5	0	MCA disabled	
		1	MCA enabled	
	D4	0	Preset count not reached	
		1	*Preset Count reached, MCA stopped*	
	D3	0	GATE is enabled and is active (stopping events)	FW6.06.07 and later
		1	GATE is disabled or GATE is inactive (not stopping events)	
	D2	0	Oscilloscope data not ready	
		1	Oscilloscope data ready	
	D1	0	Unit has not been configured	
		1	Unit is configured	
	D0	0	TBD	
36	D7	0	Auto Input Offset locked	
		1	Auto Input Offset searching	
	D6	0	MCS not finished	
		1	*MCS finished*	
	D5	0	No reboot	FW6.05 and later
		1	This is first status packet since reboot occurred	
	D4-D2	0	TBD	
	D1	0	FPGA clock = 20MHz	(formerly status of MCA RAM test, which is now in Diagnostic Packet)
		1	FPGA clock = 80MHz	
	D0	0	FPGA clock was explicitly set with 'CLCK=20' or 'CLCK=80'	
		1	'CLCK=AUTO' was used to select FPGA clock	
37	D7-D4	0	TBD	
	D3-D0	0-15	Firmware Build Number	FW6.06 and later

38	D7	0	PC5 not detected at power-up	DP5G: PC5G not detected PX5: HV Jumper error
		1	PC5 detected at power-up	DP5G: PC5G detected PX5: Normal
	D6	0	PC5/PX5 HV polarity = negative	DP5G: N/A
		1	PC5/PX5 HV polarity = positive	DP5G: N/A
	D5	0	PC5/PX5 preamp supply = +/-5V	DP5G: N/A
		1	PC5/PX5 preamp supply = +/-8.5V	DP5G: N/A
	D4-D0	0	TBD	
39	D7-D0	0	Device ID: DP5	
		1	Device ID: PX5	
		2	Device ID: DP5G	
		3	Device ID: MCA8000D	
		4	Device ID: TB5	
40	D7-D0	0-15	PX5 TEC voltage, MSB	TEC (V) = (MSB*256 + LSB) / 758.5
41	D7-D0	0-255	PX5 TEC voltage, LSB	
42 [PX5]	D7	0	TBD	
	D6		State of AUX3 input, for 'AU34=2"	FW6.08.04 and later
	D5	0	HV inhibited	These only apply if D3-D0 non-zero (i.e. a PX5 option is installed). Otherwise, both bits are zero.
		1	HV not inhibited	
	D4	0	Active-low inhibit selected	
		1	Active-high inhibit selected	
	D3-D0	0	PX5: no options installed	
		1	PX5: HPGe HVPS installed	
		2-15	TBD	
42 [MCA8000D]	D7	0	Earlier than Rev E	[FW6.08.03 and later]
		1	Rev E0 or later	
	D6-D3		TBD	
	D3-D0	0	No MCA8000D options	
		1	MCA8000D option 'PA' calibration available	
42 [DP5G]	D7-D0	0	No options	
		1	Negative HV supply installed	
42 [DP5]	D7-D0	0	TBD	
43	D7-D4	0	TBD	
	D3	0	Normal List-mode operation	
		1	Deadtime correction feature enabled	[FW6.08.02 and later] See 'LMMO' command
	D2	0	List-mode clock: 100nS	100uS in 'NOTIMETAG' mode
		1	List-mode clock: 1uS	1mS in 'NOTIMETAG' mode
	D1-D0	0	List-mode sync: INT	See 'SYNC' command

		1	List-mode sync: NOTIMETAG	[FW6.06.06 and later]
		2	List-mode sync: EXT	
		3	List-mode sync: FRAME	
44	D1-D0	0-3	DP5 AN_IN MSB	AN_IN(V) = (MSB*256 + LSB) / 419.7 (AN_IN is on J5.11) [FW6.06.07 and later]
45	D7-D0	0-255	DP5 AN_IN LSB	
46	D7-D2	0	TBD	
	D1	0	Sequential buffering is finished or disabled	[FW6.08.00 and later]
		1	Sequential buffering is running	[FW6.08.00 and later]
	D0	0-1	Current sequential buffer MSB	[FW6.08.00 and later]
47	D7-D0	0-255	Current sequential buffer LSB	[FW6.08.00 and later]
48	D7-D0	0		[FW6.08.02 and earlier]
		0xFF	Original bootloader	[FW6.08.03 and later]
		0x80	Bootloader 7.00.00	[FW6.08.03 and later]
		0x7F	Bootloader 7.00.01	[FW6.08.03 and later]
49	D7-D0	0-255	ECO byte	[FW6.08.04 and later] DP5 Rev C and earlier: = 255 DP5 Rev D and later: D7-D6=0 Rev Dx D7-D6=1 Rev Ex D7-D6=2 Rev Fx D7-D6=3 Rev Gx D5-D4=0 Rev x0 D5-D4=1 Rev x1 D5-D4=2 Rev x2 D5-D4=3 Rev x3 D3-D0=0 Configuration A … D3-D0=15 Configuration P --- DP5G, TB-5: 0 or 255=20MHz operation only DP5G, TB-5: 1=20MHz or 80Mz operation DP5G/ TB-5: 2=CLYC
50-63	D7-D0	0	N/A (Currently unused)	

4.2.2 Response packet: "256-channel spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-773	774	775
Value	0xF5	0xFA	**0x81**	**0x01**	3	0	Spectrum Data	varies	

4.2.3 Response packet: "256-channel spectrum plus Status"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field		CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-773	774-837	838	839
Value	0xF5	0xFA	**0x81**	**0x02**	3	0x40	Spectrum Data	Status Data	varies	

4.2.4 Response packet: "512-channel spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-1541	1542	1543
Value	0xF5	0xFA	**0x81**	**0x03**	6	0	Spectrum Data	varies	

4.2.5 Response packet: "512-channel spectrum plus Status"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field		CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-1541	1542-1605	1606	1607
Value	0xF5	0xFA	**0x81**	**0x04**	6	0x40	Spectrum Data	Status Data	varies	

4.2.6 Response packet: "1024-channel spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-3077	3078	3079
Value	0xF5	0xFA	**0x81**	**0x05**	0x0C	0	Spectrum Data	varies	

4.2.7 Response packet: "1024-channel spectrum plus Status"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field		CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-3077	3078-3141	3142	3143
Value	0xF5	0xFA	**0x81**	**0x06**	0x0C	0x40	Spectrum Data	Status Data	varies	

4.2.8 Response packet: "2048-channel spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-6149	6150	6151
Value	0xF5	0xFA	**0x81**	**0x07**	0x18	0	Spectrum Data	varies	

4.2.9 Response packet: "2048-channel spectrum plus Status"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field		CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-6149	6150-6213	6214	6215
Value	0xF5	0xFA	**0x81**	**0x08**	0x18	0x40	Spectrum Data	Status Data	varies	

4.2.10 Response packet: "4096-channel spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-12293	12294	12295
Value	0xF5	0xFA	**0x81**	**0x09**	0x30	0	Spectrum Data	varies	

4.2.11 Response packet: "4096-channel spectrum plus Status"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field		CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-12293	12294-12357	12358	12359
Value	0xF5	0xFA	**0x81**	**0x0A**	0x30	0x40	Spectrum Data	Status Data	varies	

4.2.12 Response packet: "8192-channel spectrum"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-24581	24582	24583
Value	0xF5	0xFA	**0x81**	**0x0B**	0x60	0	Spectrum Data	varies	

4.2.13 Response packet: "8192-channel spectrum plus Status"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field		CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-24581	24582-24645	24646	24647
Value	0xF5	0xFA	**0x81**	**0x0C**	0x60	0x40	Spectrum Data	Status Data	varies	

Purpose: These response packets are sent by the DP5 in response to a request for spectrum data – the specific response packet returned depends on how many channels the DP5's MCA is configured for, and whether the request was for spectrum data only, or spectrum plus status data.

Data Format: Spectrum data is 3 bytes/channel, LSB to MSB, starting with channel 0, up to the maximum channel number. (i.e. in 256 channel mode, the channel data goes from channel 0 to channel 255.) The status data follows the spectrum data in the Response Packet data field and is 64 bytes in length. The format is the same as is specified for the 'Status' response packet.

4.2.14 Response packet: "2048-byte Scope Packet"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-2053	2054	2055
Value	0xF5	0xFA	**0x82**	**1**	8	0	Scope data	Varies	

4.2.15 Response packet: "2048-byte Scope Packet w/ Overflow"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-2053	2054	2055
Value	0xF5	0xFA	**0x82**	**3**	8	0	Scope data	Varies	

Purpose: These response packets are returned in response to a 'Request Digital Scope Data' packet (PID1=3, PID2=1). Only one is returned – the second one (PID2=3) is returned if the Scope Gain is set to 4 or 16, and the signal strayed outside the gain range during the scope acquisition. Otherwise, the first one (PID2=1) is returned. In either case, the data is identical. (This second type is used for noise measurements.) [See the ASCII commands DACO, SCOE, SCOT & SCOG for information on configuring the Digital Scope].

Data Format: The data field contains 2048 bytes of scope data, where each byte is a single 8-bit sample from the scope. The Digital Scope captures the most significant 8 bits of digital data that is being output on the output DAC.

The timebase for the scope is dependent on the FPGA clock and the peaking time selected, as listed below. (The timebase listed is the interval between samples.)

FPGA Clock=20MHz		FPGA Clock=80MHz	
Peaking Time	**Scope Timebase**	**Peaking Time**	**Scope Timebase**
0.800 - 6.40uS	50nS	0.200 - 1.600uS	12.5nS
6.60 - 12.80uS	100nS	1.650 - 3.200uS	25nS
13.20 - 25.60uS	200nS	3.30 - 6.40uS	50nS
26.40 - 51.20uS	400nS	6.60 - 12.80uS	100nS
52.80 - 102.4uS	800nS	13.20 - 25.60uS	200nS

4.2.16 Response packet: "512-byte Misc Data Packet"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-517	518	519
Value	0xF5	0xFA	**0x82**	**2**	2	0	Misc data	Varies	

Purpose: This response packet is returned in response to a 'Request Misc Data' packet (PID1=3, PID2=2). [See the 'Write Misc Data' Request Packet for information on writing the Misc Data.]

Data Format: The data field contains 512 bytes, which is the Misc Data programmed via a 'Write Misc Data' request packet. The data can be binary, ASCII, etc. This is stored in non-volatile memory, so it remains after the power is cycled.

4.2.17 Response packet: "Ethernet Settings"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-30	31	32
Value	0xF5	0xFA	**0x82**	**4**	0	0x19	Ethernet settings	Varies	

Purpose: This response packet is returned in response to a 'Request Ethernet Settings' packet (PID1=3, PID2=4).

Data Format: The data field contains 23 bytes of Ethernet Settings, in the following format:

Offset	Value
0	0 = Use fixed IP address; 0xFF = Get IP address from DHCP server
1-4	IP Address (MSB…LSB)
5-8	IP Subnet Mask (MSB…LSB)
9-12	IP Gateway Address (MSB…LSB)
13-16	Reserved
17-18	Port (MSB,LSB: fixed at 10001 for now)
19-24	DP5 MAC Address

4.2.18 Response packet: "Diagnostic Data"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-261	262	263
Value	0xF5	0xFA	**0x82**	**5**	1	0	Diagnostic Data	Varies	

Purpose: This response packet is returned in response to a 'Request Diagnostic Data' Request Packet (PID1=3, PID2=5).

Data Format: The data field contains 256 bytes of various types of diagnostic data, in the following format: [Note: PX5 & DP5G bytes 5-38 are different!]

Offset	Bits	Value	Comment
0	D7-D4	Firmware (major)	6.0 for this release
	D3-D0	Firmware (minor)	
1	D7-D4	FPGA (major)	5.07 for this release;
	D3-D0	FPGA (minor)	0.0 indicates FPGA didn't initialize
2-4	all	SRAM error address (MSB…LSB)	0xFFFFFF indicates no error
DP5, Bytes 5-38			
5	D3-D0	DP5 board temp (raw), MSB	Temp(°C) = (MSB*256 + LSB) * 0.833 – 271.3
6	D7-D0	DP5 board temp (raw), LSB	[Offset 180 is the 8-bit signed offset cal for this]
7	D7-D0	TBD	
8	D7-D0	TBD	
9	D1-D0	Power Input, MSB	Input(V) = (MSB*256 + LSB) / 167.5
10	D7-D0	Power Input, LSB	
11	D1-D0	3.3V supply, MSB	3.3V(V) = (MSB*256 + LSB) / 254.3
12	D7-D0	3.3V supply, LSB	
13	D1-D0	2.5V supply, MSB	2.5V(V) = (MSB*256 + LSB) / 335.7
14	D7-D0	2.5V supply, LSB	
15	D1-D0	1.2V supply, MSB	1.2V(V) = (MSB*256 + LSB) / 419.7
16	D7-D0	1.2V supply, LSB	
17	D1-D0	5.5V supply, MSB	5.5V(V) = (MSB*256 + LSB) / 150.7
18	D7-D0	5.5V supply, LSB	(This is called '5.5MON' and is used in

			the -5.5V monitor below)
19	D1-D0	-5.5V supply, MSB	-5.5(V) = (MSB*256 + LSB) / 135.5 - (2.101 * 5.5MON)
20	D7-D0	-5.5V supply, LSB	
21	D1-D0	AN_IN, MSB	AN_IN(V) = (MSB*256 + LSB) / 419.7 (AN_IN is on J5.11)
22	D7-D0	AN_IN, LSB	
23	D1-D0	VREF_IN, MSB	VREF_IN(V) = (MSB*256 + LSB) / 419.7 (VREF_IN is a test point)
24	D7-D0	VREF_IN, LSB	
Offsets 25-38 will be zero if a PC5 is not detected			
25	D3-D0	PC5 HV Mon, MSB	HV (V) = (MSB*256 + LSB) / 2.731
26	D7-D0	PC5 HV Mon, LSB	
27	D3-D0	PC5 Det Temp, MSB	Det Temp (K) = (MSB*256 + LSB) / 13.65
28	D7-D0	PC5 Det Temp, LSB	
29	D3-D0	PC5 +PA supply, MSB	+PA (V) = (MSB*256 + LSB) / 455.1
30	D7-D0	PC5 +PA supply, LSB	
31-34	D7-D0	PC5 S/N, LSB…MSB	
35	D3-D0	DCAL, MSB	DCAL (V) = (MSB*256 + LSB) / 1365
36	D7-D0	DCAL, LSB	
37	D7	PC5 HV polarity	0 = -HV, 1=+HV
	D6	PC5 PA supply	0 = 5V preamp, 1 = 8.5V preamp
	D5-D0	N/A	
38	D7-D4	N/A	
	D3	PC5 9V supply	0 = OFF, 1 = ON
	D2	PC5 preamp supplies	0 = OFF, 1 = ON
	D1	PC5 HV supply	0 = OFF, 1 = ON
	D0	PC5 TEC supply	0 = OFF, 1 = ON
PX5, Bytes 5-38			
5	D3-D0	9V supply, MSB	9V (V) = (MSB*256 + LSB) / 304.1
6	D7-D0	9V supply, LSB	
7	D3-D0	3.3V supply, MSB	3.3V (V) = (MSB*256 + LSB) / 827.5
8	D7-D0	3.3V supply, LSB	
9	D3-D0	2.5V supply, MSB	2.5V (V) = (MSB*256 + LSB) / 1093
10	D7-D0	2.5V supply, LSB	
11	D3-D0	1.2V supply, MSB	1.2 (V) = (MSB*256 + LSB) / 1365

12	D7-D0	1.2V supply, LSB	
13	D3-D0	5V supply, MSB	5V (V) = (MSB*256 + LSB) / 545
14	D7-D0	5V supply, LSB	
15	D3-D0	-5V supply, MSB	-5V (V) = (MSB*256 + LSB) / 170.5 – 21.03
16	D7-D0	-5V supply, LSB	
17	D3-D0	+PA supply, MSB	+PA (V) = (MSB*256 + LSB) / 321.6
18	D7-D0	+PA supply, LSB	
19	D3-D0	-PA supply, MSB	-PA (V) = (MSB*256 + LSB) / 170.5 – 21.03
20	D7-D0	-PA supply, LSB	
21	D3-D0	TEC supply, MSB	TEC (V) = (MSB*256 + LSB) / 758.5
22	D7-D0	TEC supply, LSB	
23	D3-D0	HV supply, MSB	HV (V) = (MSB*256 + LSB) / 2.731
24	D7-D0	HV supply, LSB	
25	D3-D0	Detector Temperature, MSB	Det Temp (K) = (MSB*256 + LSB) / 13.65
26	D7-D0	Detector Temperature, LSB	
27	D1-D0	Board temperature (raw), MSB	Temp(°C) = (MSB*256 + LSB) * 1.024 – 271.3
28	D7-D0	Board temperature (raw), LSB	
29-38 TBD			
DP5G Bytes 5-38			
5-38	TBD		
Offsets 39-230 contain the Boot Record - Select items are listed below			
167-168		HV setting	Signed INT, MSB…LSB (in Volts)
169-170		TEC setting	Unsigned INT, MSB…LSB (in K)
171-172		Input Offset	Signed INT, MSB…LSB (in mV) [-2048 indicates default setting]
173-176		Preset Time	Unsigned LONG, MSB…LSB (0.1s/lsb)
177-178		DP5 DCAL	Unsigned INT, MSB…LSB (732uV/lsb) [PC5 DCAL takes precedence, if present]
179		PZ Correction	See the "Set PZ Correction" Request Packet for definition

180		uC Temp Calibration	See the "Set uC Temperature Calibration" Request Packet for definition
181		ADC Gain Calibration	See the "Set ADC Calibration" Request Packet for definitions
182		ADC Offset Calibration	
187		Highpass time constant	See the "Select High-Pass Time Constant" Request Packet for definition
188 [DP5] 189 [DP5G] 194 [PX5]		RS232 Baud rate	See the "Select RS232 Baud Rate" Request packet for definition
189 [DP5] 195 [PX5]		HV gain calibration	See the "Set HV Calibration" Request Packet for definition
190 [DP5] 196 [PX5]		HV offset calibration	
197 [PX5]		PZ Correction (1.6uS)	See the "Set 1.6uS PZ Correction" Request Packet for definition
191 [DP5] 190 [DP5G] 198 [PX5]		ECO byte	As of FW6.08.04, only used by DP5G: 1 = 80MHz operation supported 0 (or 255) = 20MHz only
Misc. Diagnostic Data			
231	D7-D4	TBD	
	D3-D0	Firmware Build #	Combined with offset 0 for full Firmware Major/Minor/Build version
232-255		TBD	

Text highlighted in Blue is new/modified since Rev A6 of the Programmer's Guide

4.2.19 Response packet: "Configuration Readback"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6…5+LEN	6+LEN	7+LEN
Value	0xF5	0xFA	**0x82**	**7**	varies		Configuration readback (ASCII)	varies	

Purpose: This response packet is returned in response to a 'Configuration Readback' Request Packet (PID1=0x20, PID2=3). The data field contains ASCII commands and parameters, separated by semicolons.

Data Format: The data field will contain the current ASCII configuration – it will have all the commands that were sent with the "Configuration Readback" Request Packet, except the parameters will have been replaced with the actual settings in use by the DP5. See the "Text Configuration" Request Packet, "Configuration Readback" Request packet, and the section on ASCII Commands for more details.

4.2.20 Response packet: "Netfinder Packet"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	DATA FIELD	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6…5+LEN	6+LEN	7+LEN
Value	**0xF5**	**0xFA**	**0x82**	**8**	**varies**		**Netfinder data**	**varies**	

Purpose: This is used to return the 'Netfinder' packet via the normal communications link. [Normally, the Netfinder data is returned by a dedicated TCP/IP socket.]

Data Format: The data field is formatted the same as an independent Netfinder packet, as documented in section 3.2.4.

4.2.21 Response packet: "I²C Read Data"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	DATA FIELD	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6…5+LEN	6+LEN	7+LEN
Value	**0xF5**	**0xFA**	**0x82**	**9**	**varies**		**I²C read data**	**varies**	

Purpose: This is used to return the data read by the 'I²C Transfer' Request Packet. If the Number of Bytes to Read ('NOBR') in the 'I²C Transfer' Request Packet is nonzero, and the I²C transfer was successful, then the 'I²C Read Data' Response Packet is returned, with the data field containing the bytes read by the transfer. [Note that if NOBR = 0, the DP5 will return an ACK OK packet rather than an 'I²C Read Data' packet with LEN=0.]

Data Format: The LEN value will be the same as NOBR, and the data field will contain the bytes read, in the order that they were read.

4.2.22 Response packet: "List-mode data"
Response packet: "List-mode data, FIFO full"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	DATA FIELD	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6…5+LEN	6+LEN	7+LEN
Value	**0xF5**	**0xFA**	**0x82**	**0x0A**	**varies**		**List-mode data**	**varies**	
Value	**0xF5**	**0xFA**	**0x82**	**0x0B**	**varies**		**List-mode data**	**varies**	

Purpose: This is used to return the data captured by List-mode. Each List-mode event is 16 or 32 bits in size, and the List-mode FIFO can hold 1024 32-bit records or 2048 16-bit records (i.e. 4KB). The LEN of the List-mode data packet can range from 0 (i.e. 0 records; the FIFO is empty) to 4096 (i.e. 1024 32-bit records or 2048 16-bit records; the FIFO is full.)

The two packet types (PID2=0x0A/0x0B) return identical data; the PID2=0x0B packet type is returned when the firmware detects that the FIFO was full when the List-mode Request Packet was received (i.e. events were likely lost.) Otherwise, the firmware will return a packet with PID2=0x0A. [The FIFO size may be increased in future FPGA versions; hence, the two different response packets, rather than having the application monitor the returned data size.]

If the "…FIFO full" form of the response packet is received, then the FIFO overflowed, and the most recent data was lost. (The FIFO stops accepting new data while it is full.)

Note: receiving this packet means that up to 4KB was read from the FIFO. However, if the FIFO is not full, then new events can be written into it while it is being read out. (If it was full, then the first bye read will switch it from Full to Not Full.) So, at the end of the readout, it may or may not be empty.

Note that the 'Buffer Select' feature (described below) and external sync (see Section 5.1.65) use the same input, so that only one of these features can be used. The other input is reserved for GATE.

Data Format: The data field contains between 0 and 1024 4-byte records, or between 0 and 2048 2-byte records, depending on configuration. Each record can be one of six formats; a 32-bit Event, a 32-bit Timetag, a 32-bit Frame+Timetag, a 16-bit event, a 16-bit Timetag, or a 16-bit null event. (The 'SYNC' command determines whether the Timetag or Frame+Timetag record is recorded, and whether 16-bit or 32-bit operation is selected.) The 32-bit (4 byte) or 16-bit (2 byte) record occurs in the packet data field from MSB to LSB. The fields in the record are bit-stuffed; some of them cross byte boundaries.

The 'LMMO' command can be used to assist with deadtime correction. 'LMMO=DTC' will enable the recording of PUR- or RTD-rejected events in the list-mode data, so that they can be counted to allow a more accurate input count rate to be calculated. This command also enables the recording of detector reset events in the datastream, so that the detector reset lockout can be included in the deadtime calculation. If LMMO=DTC is commanded, then events with an amplitude=0x0001 are detector resets, not real events.

[Note: for the purposes of deadtime calculation, each event tagged as piled up represents most likely two input events, possibly more.]

All records are 32 bits in size in the 32-bit modes (SYNC=INT/EXT/FRAME), or 16 bits in size in the 16-bit mode (SYNC=NOTIMETAG).

Byte 43 of the status packet can be read to determine the current List-mode configuration.

1. 32-bit Event Record: An 'event' is recorded when an input pulse passes all the acceptance criteria of the MCA; pileup reject (if enabled), RTD (if enabled), threshold and LLD, presets (if enabled), MCA enable, Detector Reset Lockout (if enabled), and Gate (if enabled).

D31	D30	D29-D16	D15-D0
0	Buffer Select	14-bit Amplitude	16-bit Timetag

D31=0 indicates that this is an Event Record.
'Buffer Select' is the state of an external digital signal:
PX5/DPG/Gammarad: The state of the AUX-1 input, if 'CON1=AUXIN1' is commanded;
DP5: The state of the AUXIN2 input.
If LMMO=DTC is commanded, then Buffer Select=1 indicates that this event was rejected by PUR or RTD logic and shouldn't be included in the spectrum.
14-bit Amplitude: The channel number (0 to 16383) of the event. If LMMO=DTC is commanded, then events with amplitude=0x0001 are detector resets, not real events.
16-bit timetag: The least-significant word of the List-mode timer, when the event occurred. 100nS or 1uS per count, depending on configuration. (See 'CLKL' command.) This is combined with the most significant bits from the most recent timetag record to determine the time that the event was recorded.

2. 32-bit Timetag: If List-mode was configured with 'SYNC=INT' (no external sync) or 'SYNC=EXT' (external sync, no frame), then every time the least significant 16 bits of the List-mode timer roll over (or the time is reset by an external sync signal), a Timetag record is recorded. It contains the most significant bits of the timer, so that the full 46 bits of the event time can be reconstructed. The most-significant timer bits of the Timetag record should be used for subsequent events (i.e. they should be combined with the least-significant bits in the Event record), until a new Timetag record appears.

D31	D30	D29-D0
1	0	30 MS bits of List-mode timer

D31=1, D30=0: Indicates this is a Timetag record.

3. 32-bit Frame+Timetag: If List-mode was configured with 'SYNC=FRAME', then every time an external sync occurs, a Frame+Timetag record is recorded. The record contains a 16-bit Frame count, and the most-significant 14-bits of the List-mode timer. Only 30 bits of the List-mode timer are utilized in this mode, so the 14 MS bits from the Frame+Timetag record are combined with the 16 LS bits in each Event record to reconstruct the event time.

D31	D30	D29-D14	D13-D0
1	1	16-bit Frame count	14-bit Timetag

D31=1, D30=1: Indicates this is a Frame+Timetag record.
16-bit Frame Count: This is incremented on the rising edge of an external Sync pulse.

4. 16-bit Event Record: If List-mode was configured with 'SYNC=NOTIMETAG' , then a 16-bit 'event' is recorded when an input pulse passes all the acceptance criteria of the MCA; pileup reject (if enabled), RTD (if enabled), threshold and LLD, presets (if enabled), MCA enable, Detector Reset Lockout (if enabled), and Gate (if enabled).

D15	D14	D13-D0
0	Buffer Select	14-bit Amplitude

D15=0 indicates that this is an Event Record.
'Buffer Select' is the state of an external digital signal:
PX5/DPG/Gammarad: The state of the AUX-1 input, if 'CON1=AUXIN1' is commanded;
DP5: The state of the AUXIN2 input.
If LMMO=DTC is commanded, then Buffer Select=1 indicates that this event was rejected by PUR or RTD logic and shouldn't be included in the spectrum.
14-bit Amplitude: The channel number (0 to 16383) of the event. If LMMO=DTC is commanded, then events with amplitude=0x0001 are detector resets, not real events.

If LMMO=DTC, then the following 16-bit formats are available with FW6.08.06 and later:

D15	D14	D13-D0
0	0	14-bit Amplitude

With LMMO=DTC and FW6.08.06 (and later), the following 3 records are inserted following each 16-bit timetag record, i.e. every 100uS/1mS:

D15	D14	D13	D12	D11-D0
0	1	0	0	12-bit count of PUR rejects

D15	D14	D13	D12	D11-D0
0	1	0	1	12-bit count of OTR/RTD rejects

D15	D14	D13	D12-D0
0	1	1	13-bit count of List Mode clock ticks during which reset lockout was active

5. 16-bit Timetag: If List-mode was configured with 'SYNC=NOTIMETAG' (16-bit mode), then there is no timetag attached to each event record, as there is in other SYNC modes. A timetag record is inserted in the data stream every 100uS or 1mS, depending on CLKL configuration.

D15	D14-D0
1	15-bit List-mode timer

D15=1: Indicates this is a Timetag record.
15 bit List-mode timer: The record is inserted every 100uS/1mS, and the 15-bit count is incremented each time. All events recorded between two timetags occurred in the 100uS/1mS interval between them.

If LMMO=DTC, then the following 16-bit formats are available with FW6.08.06 and later:

D15	D14	D13-D0
1	0	14-bit List-mode timer (as above)

With LMMO=DTC and FW6.08.06 (and later), the following record is inserted following each 16-bit timetag record, i.e. every 100uS/1mS:

D15	D14	D13-D0
1	1	14-bit fast counts

6. 16-bit Null Event: Because the List-mode FIFO is 32 bits wide, occasionally 16 bits of padding are required when a single 16-bit timetag is recorded. The 'Null Event' is 16 bits of zeroes, and should be discarded when interpreting the data stream.

   The List-mode logic combines a 16-bit timetag and 16-bit event whenever possible; at high rates, there should be few Null Events in the data stream. However, with no input counts, each timetag will have a corresponding Null Event in the data stream.

D15-D0
0x0000

4.2.23 Response packet: "MCA8000D Calibration Packet" [MCA8000D only]

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-22	23	24
Value	0xF5	0xFA	**0x82**	**0x0C**	0	9	Calibration data	Varies	

Purpose: This response packet is returned in response to a 'Request Option PA Calibration' Request Packet (PID1=3, PID2=0x0A.)

Data Format: The data field contains 17 bytes The format for the data field is given below:

Offset	Value
0	Calibration format 1 = Option PA
	Scale=1V, point #1
1-2	mV (1 LSB=100uV); MSB, LSB
3-4	Channel number; MSB, LSB
	Scale=1V, point #2
5-6	mV (1 LSB=100uV); MSB, LSB
7-8	Channel number; MSB, LSB
	Scale=10V, point #1
9-10	mV (1 LSB=1mV); MSB, LSB
11-12	Channel number; MSB, LSB
	Scale=10V, point #2
13-14	mV (1 LSB=1mV); MSB, LSB
15-16	Channel number; MSB, LSB

4.2.24 Response packet: "64-byte SCA Packet"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	Data Field	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6-69	70	71
Value	0xF5	0xFA	**0x83**	**1**	0	0x40	SCA data	Varies	

Purpose: This response packet is returned in response to a 'Request 32-bit SCA counters' Request Packet (PID1=4, PID2=1, 2 or 3.)

Data Format: The data field contains 64 bytes, which are read from the 32-bit SCA counter latches (i.e. there are 4 bytes per SCA counter.) The format for the data field is given below:

Offset	Value
0-3	SCA1 counter (LSB…MSB)
4-7	SCA2 counter (LSB…MSB)
8-11	SCA3 counter (LSB…MSB)
12-15	SCA4 counter (LSB…MSB)
16-19	SCA5 counter (LSB…MSB)
20-23	SCA6 counter (LSB…MSB)
24-27	SCA7 counter (LSB…MSB)
28-31	SCA8 counter (LSB…MSB)
32-35	SCA9 counter (LSB…MSB)
36-39	SCA10 counter (LSB…MSB)
40-43	SCA11 counter (LSB…MSB)
44-47	SCA12 counter (LSB…MSB)
48-51	SCA13 counter (LSB…MSB)
52-55	SCA14 counter (LSB…MSB)
56-59	SCA15 counter (LSB…MSB)
60-63	SCA16 counter (LSB…MSB)

4.2.25 Response packet: "Comm test - Echo packet"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	DATA FIELD	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6…5+LEN	6+LEN	7+LEN
Value	**0xF5**	**0xFA**	**0x8F**	**0x7F**	**varies**		**Echo data**	**varies**	

Purpose: This Response Packet is sent in response to the Request Packet of the same name. The LEN & DATA fields are the same as in the Request Packet.

Data Format: Whatever data is in the data field of the Request Packet is copied, byte-for-byte, into the data field of the Response packet.

4.3 Acknowledge Packets

Table 3– Text highlighted in Blue is new/modified since Rev A6 of the Programmer's Guide

Description	Support*	PID1	PID2	LEN MSB	LEN LSB	Data (optional)
OK	ALL	0xFF	0	0	0	
Sync error	ALL	0xFF	1	0	0	
PID error	ALL	0xFF	2	0	0	
LEN error	ALL	0xFF	3	0	0	
Checksum error	ALL	0xFF	4	0	0	
Bad parameter	ALL	0xFF	5	varies		ASCII command
Bad hex record (structure/chksum)	ALL	0xFF	6	0	0	
Unrecognized command	ALL	0xFF	7	varies		ASCII command
FPGA error (not initialized)	ALL	0xFF	8	0	0	
CP2201 not found	ALL	0xFF	9	0	0	
Scope data not available (not triggered)	ALL	0xFF	0x0A	0	0	
PC5 not present	ALL	0xFF	0x0B	varies		ASCII command
OK + Interface sharing request	ALL	0xFF	0x0C	0	0	
Busy - another interface is in use		0xFF	0x0D	0	0	
I2C error	6.01	0xFF	0x0E	0	0	
OK + FPGA upload address	6.06.04	0xFF	0x0F	0	3	Intel hex record: ADDR MSB, LSB, record type
Feature not supported by this FPGA version	6.06.05	0xFF	0x10	0	0	
Calibration data not present	6.07.02	0xFF	0x11	0	0	

* Initial firmware release which supports this packet type

4.3.1 Acknowledge packet: "OK"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**0**	0	0	0xFD	0x12

Purpose: This ACK packet indicates that the Request Packet was received without error, that its contents were recognized, and that the requested action was carried out. This ACK packet is only returned by Request Packets which do not request data.

4.3.2 Acknowledge packet: "OK, with Interface Sharing Request"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**0x0C**	0	0	0xFD	0x06

Purpose: This ACK packet has the same meaning as the "OK" ACK packet. In addition, another computer or interface is requesting that activity be paused so that it can gain access to the DP5. To allow it access, the application should stop sending traffic to the DP5. To maintain control (and deny it access), continue sending Request Packets. (Send 'Interface keep-alive' packets periodically, if no other periodic traffic is occurring. See the Interface section for more details.)

4.3.3 Acknowledge packet: "Sync Error"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**1**	0	0	0xFD	0x11

Purpose: This ACK packet indicates that the sync bytes in Request Packet were not correct, and therefore, the Request Packet was rejected.

Note: This error condition can only be generated via USB or Ethernet; RS232 uses the sync bytes to locate a packet in the RS232 data stream. In the absence of the sync byte pattern, no Request Packet is detected and thus no ACK packet can be returned.

4.3.4 Acknowledge packet: "PID Error"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**2**	0	0	0xFD	0x10

Purpose: This ACK packet indicates that PID1 & PID2 combination is not recognized as a valid Request Packet, and therefore, the Request Packet was rejected.

4.3.5 Acknowledge packet: "LEN Error"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**3**	0	0	0xFD	0x0F

Purpose: This ACK packet indicates that the LEN field of the Request Packet was not consistent with Request Packet type defined by the PID1 & PID2 combination. It is not recognized as a valid Request Packet, and therefore, the Request Packet was rejected.

4.3.6 Acknowledge packet: "Checksum Error"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**4**	0	0	0xFD	0x0E

Purpose: This ACK packet indicates that the checksum of the Request Packet was incorrect, and therefore, the Request Packet was rejected.

4.3.7 Acknowledge packet: "Bad Parameter"

	SYNC1	SYNC2	PID1	PID2	LEN	LEN	DATA	CHKSUM	CHKSUM

					MSB	LSB		MSB	LSB
Offset	0	1	2	3	4	5	6...5+LEN	6+LEN	7+LEN
Value	0xF5	0xFA	**0xFF**	**5**	0	varies	ASCII Command Echo	varies	

4.3.8 Acknowledge packet: "Unrecognized Command"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	DATA	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6...5+LEN	6+LEN	7+LEN
Value	0xF5	0xFA	**0xFF**	**7**	0	varies	ASCII Command Echo	varies	

4.3.9 Acknowledge packet: "PC5 Not Present"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	DATA	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6...5+LEN	6+LEN	7+LEN
Value	0xF5	0xFA	**0xFF**	**0x0B**	0	varies	ASCII Command Echo	varies	

Purpose: These ACK packets are in response to ASCII command errors – the data field will contain the ASCII command and parameter which caused the error. "Bad Parameter" means that the parameter isn't recognized or exceeds the range of the command. "Unrecognized Command" means that the 4-character command isn't recognized. "PC5 Not Present" is returned if a PC5 is not mated to the DP5, and a command requiring a PC5 is sent. (i.e. "HVSE", Set High Voltage.) [A 'Bad Parameter' ACK packet may also be returned for a malformed I2C Request Packet, in which case LEN=0.]

If an incomplete or garbled command is returned in the data field, it may mean that the ASCII Configuration Packet has structural issues. (Disallowed whitespace, missing semicolon, etc.)

4.3.10 Acknowledge packet: "Bad Hex Record"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**6**	0	0	0xFD	0x0C

Purpose: This ACK packet applies to microcontroller or FPGA upload packets (PID1=0x30, PID2=2 or 7.) It means that the hex record contained in the data field of the Request Packet had a checksum or other structural error.

4.3.11 Acknowledge packet: "FPGA Error"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**8**	0	0	0xFD	0x0A

Purpose: This ACK packet indicates that the FPGA failed initialization, and is returned in response to "Request Spectrum" (PID1=2) packets.

4.3.12 Acknowledge packet: "CP2201 Not Found"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**9**	0	0	0xFD	0x09

Purpose: This ACK packet indicates that the "Set Ethernet Settings" (PID1=0xF0, PID2=0x11) was received, but an Ethernet controller was not detected on the DP5. [Some early DP5s were manufactured without an Ethernet controller.]

4.3.13 Acknowledge packet: "Scope Data Not Available"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**0x0A**	0	0	0xFD	0x08

Purpose: This ACK packet indicates that a "Send Scope Data" (PID1=3, PID2=1 or 3) was received, but the digital oscilloscope hasn't triggered, so no data is available. [The digital oscilloscope must be armed, and then a trigger must occur for data to be available.]

4.3.14 Acknowledge packet: "I^2C Error"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**0x0E**	0	0	0xFD	0x04

Purpose: This ACK packet indicates that the I^2C Bus Master attempted a transfer as described by the 'I^2C Transfer' Request Packet, but no I^2C ACK was detected from an I^2C Slave.

4.3.15 Acknowledge packet: "Feature not supported by this FPGA version"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**0x10**	0	0	0xFD	0x02

Purpose: This ACK packet indicates that a Request Packet has been recognized as valid by the firmware, but it is not supported by the installed FPGA version. Update the FPGA to the latest FP version.

4.3.16 Acknowledge packet: "Calibration data not present"

	SYNC1	SYNC2	PID1	PID2	LEN MSB	LEN LSB	CHKSUM MSB	CHKSUM LSB
Offset	0	1	2	3	4	5	6	7
Value	0xF5	0xFA	**0xFF**	**0x11**	0	0	0xFD	0x01

Purpose: This ACK packet indicates that a Request Packet has been recognized as valid by the firmware, but that the requested calibration data has not been previously programmed into the device.

5 ASCII Commands

In the following section, the format is specified for all the ASCII commands recognized by the DP5. These commands are sent to the DP5 in the 'Text Configuration' Request Packet (PID1=0x20, PID2=2). The commands can be sent singly, but most often, they are grouped together into a single Text Configuration packet so that the entire configuration can be sent at once.

Generally, when the entire configuration is sent at once, the first command should be "RESC=Y". This resets the configuration to a known state before applying the configuration commands. This is not automatically done because it may be possible that the required configuration is larger than can be sent in a single 'Text Configuration' Request Packet. If this is the case, then "RESC=Y" and as many commands as will fit should be sent in the first Text Configuration packet, with the remaining commands in later packets. Also, it may be desirable to send individual commands to fine-tune the configuration.

This is discussed in the 'Text Configuration' Request Packet definition, but it's worth mentioning again: all ASCII characters must be upper-case; no whitespace is allowed (i.e. no spaces, tabs, CR-LF, etc.); and the commands are separated by semicolons.

Some commands have dependencies; they require other commands to be listed before them. For example, the Peaking Time command (TPEA) needs to know what FPGA clock to use, so it requires the FPGA Clock (CLCK) command to be listed before it. Likewise, many commands are dependent on the TPEA command, so it must precede them. If a dependent command is specified, that command must occur prior to the command which lists the dependency. The table below specifies the 'Order' for each command – lower Order commands must be sent before higher Order commands.

5.1 Table 4 – ASCII Command Summary

Text highlighted in Blue is new/modified since Rev A7 of the Programmer's Guide

Description	Support*	Command	Parameter	Units	Default	ORDER	Limits
Analog input pos/neg	ALL; not M	AINP	[PO{S}|NE{G}]		NEG		
Select AUX3/4 mode	6.08.04; P	AU34	[#]		1		1-2
AUX_OUT1 selection	prior to 6.08.02	AUO1	[#|ICR|PILEUP|MCSTB| ONESH|DETRES|MCAEN| PEAKH|SCA8]		ICR		1-8 or the exact strings listed
AUX_OUT1 selection	6.08.02	AUO1	[ICR|PILEUP|MCSTB| ONESH|DETRES|MCAEN| PEAKH|SCA8|RTDOS| VETO|LIVE]		ICR		The exact strings listed
AUX_OUT2 selection	prior to 6.08.02	AUO2	[#|ICR|DIAG|PEAKH| ONESH|RTDOS| RTDREJ|LIVE|VETO| STREAM]		ICR		1-9 or the exact strings listed
AUX_OUT2 selection	6.08.02	AUO2	[ICR|PILEUP|MCSTB| ONESH|DETRES|MCAEN| PEAKH|SCA8|RTDOS| VETO|LIVE|STREAM]		ICR		The exact strings listed
BLR down correction	ALL; not M	BLRD	[#]		0		0-3
BLR mode	ALL; not M	BLRM	[OF{F}|1]		OFF		only '1' for now
BLR up correction	ALL; not M	BLRU	[#]		0		0-3
Turn supplies on/off at power up	ALL; D	BOOT	[ON|OF{F}]				
Select Connector 1 signal	6.03; P, G, T	CON1	[DAC|AUXOUT1| AUXIN1]		AUXIN1 (DP5G); DAC (PX5)		
Select Connector 2 signal	6.03; P, G, T	CON2	[AUXOUT2|AUXIN2 GATEH|GATEL]		AUXIN2 (DP5G); AUXOUT2 (PX5)		
20MHz/80MHz	ALL; not M	CLCK	[AU{TO}|20|80]		AUTO ['20' for DP5G]	2	
List-mode clock	6.06.05; not M	CLKL	[100|1000]	[NS]	100		
Non-trapezoidal shaping	ALL; not M	CUSP	[OFF|##]		0% (trapezoid)		-99 to +99% (0%=trapezoid)
DAC offset	ALL; not M	DACF	[{-}###]	[MV]	0mV		-500 to +499mV
DAC output	ALL; not M	DACO	[#|OFF|FAST|SHAPED |INPUT| PEAK]		OFF		1-8
Analog gain index	ALL	GAIA	[##]				DP5: 1-16 PX5: 1-28

							DP5G: 1-4 TB-5: 1-4 MCA8000D: 1-2 DP5 Rev D: 1-24
Fine gain	ALL; not M	GAIF	[##.####]			4	0.5-1.9999
Total Gain (analog * fine)	ALL	GAIN	[###.###]			4	DP5: 0.75-150 PX5: 0.75-500 DP5: 1-10 MCA8000D: 1 or 10
Gate control	ALL; D, M	GATE	[OF{F}|HI{GH}|LO{W}]		OFF		
G.P. counter edge	ALL	GPED	[RI{SING}|FA{LLING}]		FALLING		
G.P. counter uses GATE	ALL	GPGA	[ON|OF{F}]		ON		
G.P. counter input	ALL	GPIN	[#|AUX1|AUX2|PILEUP| RTDREJ|SCA8|TBD| DETRES|OFF]		AUX1		1-8
G.P. counter cleared with MCA counters?	ALL	GPMC	[ON|OF{F}]		ON		
G.P. counter uses MCA_EN?	ALL	GPME	[ON|OF{F}]		ON		
HV set	ALL; not M	HVSE	[{+|-}####|OF{F}]	[V]	OFF		0 to 1499V (+HV); 0 to -1499V (-HV)
Input offset	ALL; D, P	INOF	[{+|-}####|AU{TO}|DE{F}]	[MV]	DEF	AINP (for DEF)	-2047 to +2047mV
Input offset gain	6.06; P	INOG	[LO{W}|HI{GH}|		LOW		
MCA/MCS channels	ALL	MCAC	[256|512|1024|2048| 4096|8192]		1024		
MCA/MCS enable	ALL	MCAE	[ON|OF{F}]		OFF (disabled)		
MCA Source	ALL	MCAS	[NO{RM}|MC{S}|FA{ST}| PU{R}|RT{D}]		NORM	6	
MCS low threshold	6.01	MCSL	[####]	[CH]	0		0-8191
MCS high threshold	6.01	MCSH	[####]	[CH]	8191		0-8191
MCS timebase	ALL	MCST	[###.###]	[S]	1.00S		0.01-655.35S
preamp 8.5/5	ALL; D, P	PAPS	DP5: [8{.5}|5|OF{F}|ON] PX5: [8{.5}|5|OF{F}]	[V]	OFF		
Preamp pole-zero cancellation	6.05; P	PAPZ	[####.#|OFF]	[US]	OFF		34.5-4387uS
Peak detect mode (min/max)	D,P,G, T	PDMD	[NORM|MIN]		NORM		
Peak detect mode	M	PDMD	[NORM|MIN|ABS|CLK|INT]		NORM		
Preset counts, low threshold	6.01	PRCL	[####]	[CH]	0		0-8191
Preset counts, high threshold	6.01	PRCH	[####]	[CH]	8191		0-8191

Preset counts	ALL	PREC	[##########|OF{F}]		OFF		0-4294967295 (2^32 -1)
Preset Livetime	6.07.00; M	PREL	[########.###|OF{F}]		OFF		0 – 4,294,967.29 s
Preset Real Time	6.01	PRER	[########.###|OF{F}]		OFF		0 – 4,294,967.29 s
Preset time	ALL; D, P, G	PRET	[#######.#|OF{F}]	[S]	OFF		0-99999999.9s
PUR interval, on/off	D,P,G	PURE	[ON|OF{F}|MAX|###.###]	[US]	OFF	4 (for ###.###)	
PUR Enable	M	PURE	[HI{GH}|LO{W}|OF{F}]		OFF		
Reset Configuration	ALL	RESC	[Y{ES}|NO]			1	
Detector Reset lockout	ALL; not M	RESL	[#####|OF{F}]	[US]	OFF	4	0-65535uS
Custom RTD oneshot delay	ALL; not M	RTDD	[###]			6	1-127 decimated clocks
RTD on/off	ALL; not M	RTDE	[ON|OF{F}]		OFF	5	
RTD sensitivity	ALL; not M	RTDS	[####]	[%]	0		2-1593
RTD threshold	ALL; not M	RTDT	[##.###]	[%]	0		0-49.9
Custom RTD oneshot width	ALL; not M	RTDW	[###]			6	1-127 decimated clocks
SCAx high threshold	ALL	SCAH	[####]		0 (all SCAs)		0-8191
SCA index	ALL	SCAI	[##] (1-16)				1-16
SCAx low theshold	ALL	SCAL	[####]		0 (all SCAs)		0-8191
SCAx output (SCA1-8 only)	ALL	SCAO	[OF{F}|HI{GH}|LO{W}]		OFF (all SCAs)		
SCA pulse width (not indexed - SCA1-8)	ALL	SCAW	[100|1000]	[NS]	100		
Scope trigger edge	ALL	SCOE	[RI{SING}|FA{LLING}]		RISING		
Digital scope gain	ALL	SCOG	[1|4|16]		1		
Scope trigger position	ALL	SCOT	[87|50|12|-25]	[%]	87%		
Set scintillator time constant	6.08.01; G, T	SCTC	[####|OF{F}]	[NS]	OFF	4	0-1599nS
Set spectrum offset	ALL	SOFF	[OFF|{-}####.###]	[CH]	OFF	after MCAC	-8192 to +8191.75 (8K channels); -4096 to +4095.875 (4K channels)…
List-mode sync source	6.06.05; not M	SYNC	[IN{T}|EX{T}|FR{AME}|NO{TIMETAG}]		INT		
TEC set	ALL; D, P	TECS	[###|OF{F}]	[K]	OFF		0-299K
Flat top	ALL; not M	TFLA	[##.###]	[US]	0uS	4	0-51.2uS
Fast threshold	ALL; not M	THFA	[###.###]		0		0-255.937
Slow threshold	ALL	THSL	[##.###]	[%]	0		0-24.9%

LLD threshold	6.01	TLLD	[####|OF{F}]	[CH]	OFF		0-8191
Peaking time	ALL; not M	TPEA	[###.###]	[US]	no default	3	0.8-102.4uS (CLK=20MHz); 0.05-25.6uS (80MHz); 0.05-102.4uS (AUTO)
Fast channel peaking time	ALL; not M	TPFA	[50|100|200|400|1600]	[NS]	100 (80MHz); 400 (20MHz)	4	50, 100, 400 (80MHz); 200, 400, 1600 (20MHz)
Fast channel peaking time	6.07.05; not M	TPFA	[50|100|200|400| 800|1600|3200]	[NS]	100 (80MHz); 400 (20MHz)	4	50,100,200,400, 800 (80MHz); 200,400,800, 1600,3200 (20MHz)
Test pulser on/off	ALL; not M	TPMO	[OF{F}|+S{NG}|+D{BL}| -S{NG}|-D{BL}]		OFF		
Volume [PX5 only]	ALL; P	VOLU	[OF{F}|ON]		OFF		

*Support: Minimum firmware (FW) version to support command, plus which devices support it;
'D' = DP5; 'P' = PX5, 'G' = DP5G (GammaRad), 'T' = TB-5, 'M' = MCA8000D. If none are listed, then all 5 devices support the command

5.1.1 AINP - Set the Input Polarity

Command: AINP
Parameter: [PO{S}|NE{G}]
Units: none
Default: NEG

Dependencies: none
Supported: FW6.00 and later
Related: INOF

Description: AINP selects the polarity of the pulses at the DP5 signal input. An Amptek Si-PIN detector produces negative-going steps; the AINP setting is 'NEG'. An Amptek SDD detector produces positive-going steps; the AINP setting 'POS'. [The AINP command is not related to the voltage polarity of the input; it is used for selecting the polarity of the input pulses.]

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of those listed.

Example: AINP=POS; // Select +input pulses for SDD

5.1.2 AU34 - Select AUX3/4 Mode [PX5 only]

Command: AU34
Parameter: [#]

Units: none
Default: 1
Range: 1-2

Dependencies: none
Supported: FW6.08.04 and later (PX5 only)

Description: AU34 selects the mode for the AUX3 and AUX4 signals on the PX4, as follows:
'1': AUX3 and AUX4 are outputs; AUX3 outputs the same signal as AUX_OUT1; AUX4 outputs the same signal as AUX_OUT2
'2': AUX3 is an input, and AUX4 is an output, which generates 25mS pulses. This mode is for use with a 'sample changer'.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified.

Example: AU34=1; // Set the AUX3 & AUX4 to outputs

5.1.3 AUO1 - Select AUX_OUT1 Signal

Command: AUO1
Parameter: [#|ICR|PILEUP|MCSTB|ONESH| DETRES|MCAEN|PEAKH|SCA8] (prior to 6.08.02)
Parameter: [ICR|PILEUP|MCSTB|ONESH| DETRES|MCAEN|PEAKH|SCA8
RTDOS|RTDREJ|VETO|LIVE] (6.08.02 and later)
Units: none
Default: ICR
Range: 1-8 or the exact strings listed ('1-8' removed in 6.08.02 and later)

Dependencies: none
Supported: FW6.00 and later (see above notes)
Related: SCOE, SCOT, CON1 (PX5/DP5G)

Description: AUO1 selects the source for the AUX_OUT1 signal. The selected signal is also used as the trigger source for the digital oscilloscope. [Note that PX5 and DP5G require the 'CON1' command in order to connect the AUXOUT1 signal to the AUX1 connector.]

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified, in which case the default of ICR will be used. [Most of the commands which have text parameters only require the first two characters; this command requires all characters specified.]

Example:
```
AUO1=PILEUP;          // Set the AUX_OUT1 signal to PILEUP,
                      // and trigger the digital scope on it
```

5.1.4 AUO2 - Select AUX_OUT2 Signal

Command: AUO2
Parameter: [#|ICR|DIAG|PEAKH|ONESH|RTDOS|RTDREJ|LIVE|VETO|STREAM] (prior to 6.08.02)
Parameter: [ICR|PILEUP|MCSTB|ONESH| DETRES|MCAEN|PEAKH|SCA8 RTDOS|RTDREJ|VETO|LIVE|STREAM] (6.08.02 and later)
Units: none
Default: ICR
Range: 1-9 or the exact strings listed, for FW6.06.06 and later
1-8 or the exact strings listed, except for 'STREAM', prior to FW6.06.06
The exact strings listed, for FW6.08.02 and later

Dependencies: none
Supported: FW6.00 and later (FW6.02 and later for string names, FW6.06.06 for 'STREAM')
Related: CON2 (PX5/DP5G)

Description: AUO2 selects the source for the AUX_OUT2 signal. . [Note that PX5 and DP5G require the 'CON2' command in order to connect the AUXOUT2 signal to the AUX2 connector.]

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified, in which case the default of ICR will be used. [Most of the commands which have text parameters only require the first two characters; this command requires all characters specified.]

Example: AUO2=RTDOS; // Set the AUX_OUT2 signal to RTDOS

5.1.5 BLRD - Select the Baseline Restorer 'Down' Correction

Command: BLRD
Parameter: [#]
Units: none
Default: 0
Range: 0-3
0-5 [FW6.09.02/FP6.14 and later]

Dependencies: none
Supported: FW6.00 and later
Related: BLRM, BLRU

Description: BLRD selects the size of the BLR 'down' correction. '0' is the smallest (slowest, least aggressive) and '3' is the largest (fastest, most aggressive.) With FW6.09.02, the largest setting is increased to '5', which helps with microphonics, cosmic rays, and other events that produce unusually large baseline disturbances.

Errors: An INVALID PARAMETER error will be returned if the parameter is not in the *range* specified.

Example:
```
BLRD=3;          // Select the most aggressive BLR 'down'
                 // correction
```

5.1.6 BLRM - Select the Baseline Restorer Mode

Command: BLRM
Parameter: [OF{F}|1]
Units: none
Default: OFF

Dependencies: none
Supported: FW6.00 and later
Related: BLRU, BLRD

Description: BLRM selects whether the Baseline Restorer is enabled, and if so, which mode it will operate in. In the initial release (FW6.00), only BLR mode 1 is supported; others will be added in the future.

Errors: An INVALID PARAMETER error will be returned if the parameter is not 'OFF' or '1'.

Example: BLRM=1; // Enable the BLR

5.1.7 BLRU - Select the Baseline Restorer 'Up' Correction

Command: BLRU
Parameter: [#]
Units: none
Default: 0
Range: 0-3

Dependencies: none
Supported: FW6.00 and later
Related: BLRM, BLRD

Description: BLRU selects the size of the BLR 'up' correction. '0' is the smallest (slowest, least aggressive) and '3' is the largest (fastest, most aggressive.)

Errors: An INVALID PARAMETER error will be returned if the parameter is not in the *range* specified.

Example: BLRU=1; // Select the 2nd slowest BLR 'up' correction

5.1.8 BOOT - Set Power-on State

[DP5]

Command: BOOT
Parameter: [ON|OF{F}]
Units: none
Default: none

Dependencies: none
Supported: FW6.00 and later; DP5 only [not supported by PX5 or DP5G – for PX5, power button is held in at power-up to start with power supplies on. DP5G/PCG always boots with HV DAC set to its previous state.]
Related: HVSE, PAPS, TECS

Description: BOOT determines whether the PC5 power supplies (HV, TEC & Preamp) will be turned on automatically when power is applied to the DP5/PC5. If this is set to 'ON', then the next time the DP5/PC5 is powered up, the HV, TEC & Preamp supplies will automatically be set to the previously applied settings. The 'BOOT' setting is non-volatile; its setting will be retained and is not reset by the Reset Configuration ("RESC") command. Therefore, it only needs to be sent once, although there is no harm in including it with each configuration.

Errors: An INVALID PARAMETER error will be returned if the parameter is not 'ON' or 'OFF'.

Example: BOOT=ON; // Turn on the PC5 supplies at power-up

5.1.9 CON1 – Select signal for AUX1 Connector

[PX5 & DP5G]

Command: CON1
Parameter: [DAC|AUXOUT1|AUXIN1]
Units: none
Default: DAC (PX5); AUXIN1 (DP5G)

Dependencies: none
Supported: FW6.03 and later; PX5 and DP5G [DP5 uses DACO, AUO1 & AUO2 to select signals. PX5 & DP5G use CONx commands to route selected signals to external connectors.]
Related: CON2, DACO, AUO1, AUO2, GPIN

Description: Selects the signal for the AUX1 connector on PX5 or DP5G/PCG. 'DAC' routs the output DAC to the AUX1 connector. ('DACO' selects which signal the DAC will output.) 'AUXOUT1' will output the digital signal selected by the 'AUO1' command. 'AUXIN1' switches the AUX1 connector to an input – 'AUXIN1' can then be selected as an input to the General Purpose Counter (via GPIN).

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the options specified.

Example: CON1=AUXOUT1; // Configure Connector 1 to AUXOUT1

5.1.10 CON2 – Select signal for AUX2 Connector

[PX5 & DP5G]

Command: CON2
Parameter: [AUXOUT2|AUXIN2|GATEH|GATEL]
Units: none
Default: AUXOUT2 (PX5); AUXIN2 (DP5G)

Dependencies: none
Supported: FW6.03 and later; PX5 and DP5G [DP5 uses DACO, AUO1, AUO2 & GATE to select signals. PX5 & DP5G use CONx commands to route selected signals to external connectors.]
Related: CON1, AUO1, AUO2, GPIN, GATE

Description: Selects the signal for the AUX2 connector on PX5 or DP5G/PCG. 'AUXOUT2' will output the digital signal selected by the 'AUO2' command. 'AUXIN2' switches the AUX1 connector to an input – 'AUXIN2' can then be selected as an input to the General Purpose Counter (via GPIN). 'GATEH' or 'GATEL' switches the AUX2 connector to an input, and uses the AUX2 signal as an active-high or active-low gate input. "GATEH" means that events are rejected while the GATE input is high; "GATEL" means that events are rejected while the GATE input is low.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the options specified.

Example: CON2=AUXOUT2; // Configure Connector 2 to AUXOUT2

5.1.11 CLCK - Select FPGA Clock

Command: CLCK
Parameter: [20|80|AU{TO}] [DP5/PX5]
[20] [DP5G]
Units: MHZ
Default: AUTO [DP5/PX5]
20 [DP5G]

Dependencies: none
Supported: FW6.00 and later
Related: TPEA

Description: CLCK sets the FPGA clock to either 20MHz or 80MHz. If 'AUTO' is used as the parameter, then the value of the peaking time command (TPEA) will determine whether the FPGA clock is 20MHz or 80MHz. [The DP5G only supports 20MHz operation].

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of those listed.

Example: CLCK=20; // This sets the FPGA clock to 20MHz

5.1.12 CLKL - Select List-Mode Clock

Command: CLKL
Parameter: [100|1000]
Units: NS (normal), or US for 16-bit List Mode
Default: 100

Dependencies: none
Supported: FW6.06.05 and later
Related: SYNC

Description: CLKL selects the clock period (i.e. resolution) for the List-mode timer. It can be set to either 100nS or 1000nS (1uS). For 16-bit List-mode operation (SYNC=NOTIMETAG), this sets the timetag interval to 100uS or 1000uS (1mS). See Section 6.1.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of those listed.

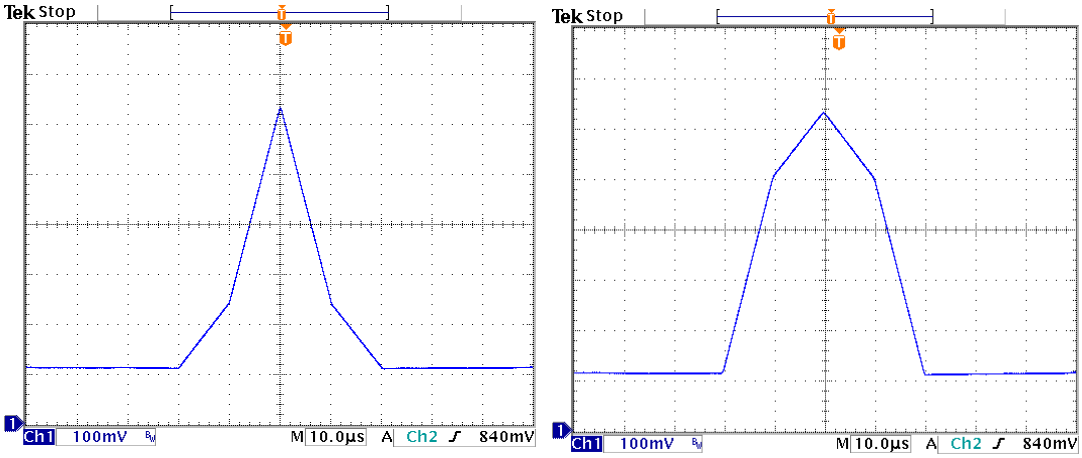
Example: CLKL=1000; // This sets the List-mode clock to 1uS

5.1.13 CUSP - Specify Non-Trapezoidal Shaping

Command: CUSP
Parameter: [{+|-}##|OF{F}]
Units: %
Default: OFF (same as 0%)
Range: -99 to +99; ~3.1% precision

Dependencies: none
Supported: FW6.00 and later
Related: TPEA

Description: CUSP determines whether the shaper produces a trapezoidal pulse shape (CUSP=0% or OFF); a cusp-like shape (parameter is positive); or a Gaussian-like shape (parameter is negative.) Below are scope captures, with Peaking Time set to 20uS and Flat Top set to 0uS; on the left is CUSP=+50%. On the right is CUSP=-50%.



Errors: An INVALID PARAMETER error will be returned if the parameter is a number outside the specified range. A text parameter is the same as OFF and will not return an error.

Example: CUSP=50; // Enable cusp-like shaping with 50% depth

5.1.14 DACF - Set DAC Offset

Command: DACF
Parameter: [{+|-}###]
Units: MV (millivolts)
Range: -500 to +499 mV (~3.9mV precision)
Default: 0mV

Dependencies: none
Supported: FW6.00 and later
Related: DACO, TPMO

Description: DACF sets the offset for the output DAC. The DAC has on output range of 0-1V – changing the offset allows one to see signals that would otherwise be out of range of the DAC. With a setting of 0, the DP5 clamps signals below 0V to 0V, and above 1V to 1V. At other DACF settings, the signal wraps around. [Note: if the test pulser function is enabled, then this command sets the amplitude of the test pulse. See TPMO for details.]

Errors: An INVALID PARAMETER error will be returned (and the DAC offset set to 0) if the commanded threshold is outside the range given.

Example:
```
DACF=30;    // This sets the DAC offset to 30mV, to allow signals
            // slightly below logical ground to be seen.
```

5.1.15 DACO - Select Signal for Output DAC

Command: DACO
Parameter: [#|OFF|FAST|SHAPED|INPUT|PEAK]
Units: none
Default: OFF
Range: 1-8, if a number is specified

Dependencies: none
Supported: FW6.00 and later
Related: DACF, CON1 (PX5/DP5G)

Description: DACO selects the signal to be output via the DAC. Generally, this is used for diagnostic purposes – the various signals can be inspected on an oscilloscope. Either the signal name can be used, or an index number, starting with 1 = 'FAST'. The selected signal is also fed into the Digital Oscilloscope. (See SCOE, SCOT and SCOG). Note: if the Test Pulser function is enabled, the DAC will output the test pulse signal while the Digital Oscilloscope will continue to capture the selected signal. **Note: PX5 and DP5G require the 'CON1' command to connect the output DAC to the AUX1 connector.**

Errors: An INVALID PARAMETER error will be returned if the parameter is not 1-8, or the signal name exactly as listed. [Most of the commands which have text parameters only require the first two characters; this command requires all characters specified.]

Example:
```
DACO=SHAPED;        // Select the shaped channel for the
                    // output DAC
```

5.1.16 GAIA - Set the Analog Gain Index

Command: GAIA
Parameter: [##]
Units: none
Default: none
Range: 1 to 16 [DP5]
1 to 28 [PX5]
1 to 4 [DP5G]
1 to 24 [DP5 Rev D]
1 to 2 [MCA8000D]

Dependencies: none
Supported: FW6.00 and later
FW6.09.00 and later [DP5 Rev D]
Related: GAIF, GAIN

Description: GAIA selects the analog gain. The parameter specified is an index; it selects the analog gain from the list below. The first one listed has an index of 1, up to the last one, which has an index of 16 (DP5), 28 (PX5), or 4 (DP5G).

Available DP5 analog gains: 1.12, 2.49, 3.78, 5.28, 6.56, 8.39, 10.09, 11.32, 14.55, 17.77, 22.40, 30.84, 38.12, 47.47, 66.16, 101.83

Available DP5 Rev D analog gains: 1.00, 1.25, 1.56, 1.95, 2.43, 3.04, 3.80, 4.75, 5.98, 7.47, 9.34, 11.67, 14.61, 18.25, 22.82, 28.52, 35.53, 44.39, 55.52, 69.37, 87.27, 109.04, 136.36, 170.38

Available PX5 analog gains: 1.00, 1.25, 1.56, 1.95, 2.43, 3.04, 3.78, 4.75, 5.96, 7.47, 9.34, 11.66, 14.57, 18.18, 22.72, 28.37, 35.46, 44.64, 55.83, 69.79, 87.10, 108.62, 135.84, 169.80, 211.99, 264.99, 330.70, 413.38

Available DP5G analog gains: 1.57, 2.56, 4.09, 6.77

Available MCA8000D analog gains: 1V full-scale, 10V full-scale

Errors: An INVALID PARAMETER error will be returned if the parameter is not with the *range* specified.

Example: GAIA=5; // Select an analog gain of 6.56 (DP5)

5.1.17 GAIF - Set the Fine Gain

Command: GAIF
Parameter: [##.####]
Units: none
Default: none
Range: 0.5-1.9999

Dependencies: TPEA must precede GAIF
Supported: FW6.00 and later
Related: GAIA, GAIN

Description: GAIF sets the fine gain. The total gain is a product of the analog gain and fine gain. [Generally, either the GAIN command is used, or the combination of GAIA and GAIF.]

Internally, the fine gain is combined with a normalization for gain variations due to peaking time. Because of this, the precision of the fine gain is dependent on peaking time. It is always has a precision of at least 1 channel in 8192; generally, the precision is better than that.

Errors: An INVALID PARAMETER error will be returned if the parameter is not with the *range* specified.

Example: GAIF=1.05; // Set the digital fine gain to 1.05

5.1.18 GAIN - Set the Total Gain

Command: GAIN
Parameter: [###.###]
Units: none
Default: none
Range: 0.75 to 150 [DP5]
0.75 to 500 [PX5]
1.0 to 10.0 [DP5G]
1 or 10 [MCA8000D]
0.75 to 250 [DP5 Rev D]

Dependencies: TPEA must precede GAIN
Supported: FW6.00 and later
Related: GAIA, GAIF

Description: GAIN sets the total gain. First, it searches for the nearest available 'coarse gain' for the analog front end (listed below for reference.) It then calculates the digital 'fine gain' to achieve the commanded gain, while also normalizing for gain differences caused by peaking time variations.

(See the GAIA command for available analog gains)

For the MCA8000D, there are only two valid settings: '1' (1V full-scale), or '10' (10V full-scale).

Errors: An INVALID PARAMETER error will be returned if the parameter is not with the *range* specified.

Example: GAIN=100; // Set the combined digital and analog gain to 100

5.1.19 GATE - Configure the GATE Input

[DP5 & MCA8000D]

Command: GATE
Parameter: [OF{F}|HI{GH}|LO{W}]
Units: none
Default: OFF

Dependencies: none
Supported: FW6.00 and later; DP5 & MCA8000D only [PX5 and DP5G use 'CON2' to configure the GATE function]
Related: CON2 (PX5 & DP5G)

Description: GATE selects whether the GATE function is enabled, and if so, the polarity of the GATE input. For the DP5, "HIGH" means that events are rejected while the GATE input is high; "LOW" means that events are rejected while the GATE input is low. **If enabled, GATE uses the DP5 AUX_IN1 input, which has a pull-down resistor on it**. **The MCA8000D uses GATE1 as the GATE input, and this has a weak pull-up resistor**

For the MCA8000D, "HIGH" means that events are accepted while the GATE input is high; "LOW" means that events are accepted while the GATE input is low. [This is actually the opposite polarity that was intended. The polarity can be reversed in FW6.09.00 (and later) by using Firmware Manager to set ECO=1]

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified.

Example:
```
GATE=HIGH;      // Enable GATE – events are rejected while input
                // is high
```

5.1.20 GPED - Select General Purpose Counter Edge

Command: GPED
Parameter: [RI{SING}|FA{LLING}]
Units: none
Default: FALLING

Dependencies: none
Supported: FW6.00 and later
Related: GPIN, GPME, GPGA, GPMC; 'Clear G.P. Counter' Request Packet

Description: GPED selects on which edge of its source the General Purpose (G.P.) Counter will increment.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified.

Example: GPED=RI; // Count on the rising edge of the G.P. Counter input

5.1.21 GPGA - General Purpose Counter Uses GATE

Command: GPGA
Parameter: [ON|OF{F}]
Units: none
Default: ON

Dependencies: none
Supported: FW6.00 and later
Related: GPED, GPIN, GPME, GPMC, GATE; 'Clear G.P. Counter' Request Packet

Description: GPGA selects whether the G.P. counter is conditioned by the GATE input. In order to use this, the GATE command must also be sent to configure the GATE input polarity. If GATE is disabled ('GATE=OFF'), then GPGA will have no effect. GPGA is redundant if GPME=ON, because MCA Enable is gated by GATE already.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified.

Example: GPGA=ON; // Qualify the G.P. Counter with GATE

5.1.22 GPIN - Select the Source for the General Purpose Counter

Command: GPIN
Parameter: [#|AUX1|AUX2|PILEUP|RTDREJ|SCA8|RESPER|DETRES|OFF]
Units: none
Default: AUX1
Range: 1-8

Dependencies: none
Supported: FW6.00 and later; 'RESPER' FW6.07.05 and later
Related: GPED, GPME, GPGA, GPMC; 'Clear G.P. Counter' Request Packet; CON1, CON2 (PX5/DP5G)

Description: GPIN selects the source for the General Purpose (G.P.) Counter. The G.P. Counter will count rising or falling edges of the source (see GPED). ('AUX1' refers to the DP5 AUX_IN1 input; 'AUX2 ' refers to the DP5 AUX_IN2 input. 'TBD' is currently undefined.) An index can be used rather than the signal name; 1=AUX1…8=OFF. Note: PX5 and DP5G require the 'CON1' ('CON2') command to connect the AUXIN1 (AUXIN2) input to the AUX1 (AUX2) connector, for it to be available as a counter source.

'RESPER' is used the measure the detector reset period. In this mode, the lower 2 bytes of the GP Counter record the most recent reset period, at 1mS/count, to a maximum of 65.535 seconds. [The counter will stop at 65.535s if it reaches this, rather than rolling over.] The upper 2 bytes are 0.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified, or a number in the range specified, in which case the default of AUX1 will be used. [Most of the commands which have text parameters only require the first two characters; this command requires all characters specified.]

Example:
```
GPIN=RTDREJ;        // Set the G.P. Counter to count events
                    // rejected by RTD
```

5.1.23 GPMC - General Purpose Counter is Cleared with MCA

Command: GPMC
Parameter: [ON|OF{F}]
Units: none
Default: ON

Dependencies: none
Supported: FW6.00 and later
Related: GPED, GPIN, GPME, GPGA, GATE; 'Clear G.P. Counter' Request Packet

Description: GPMC selects whether the G.P. counter is cleared when the MCA (spectrum) is cleared. If GPMC=OFF, then the G.P. Counter is only cleared by the 'Clear G.P. Counter' Request Packet.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified.

Example:
```
GPMC=ON;        // Clear the G.P. Counter when the spectrum is
                // cleared
```

5.1.24 GPME - General Purpose Counter Uses MCA Enable

Command: GPME
Parameter: [ON|OF{F}]
Units: none
Default: ON

Dependencies: none
Supported: FW6.00 and later
Related: GPED, GPIN, GPGA, GPMC; 'Clear G.P. Counter' Request Packet

Description: GPME selects whether the G.P. Counter is gated by the internal MCA Enable signal, or whether it is free-running. [The MCA is disabled by Detector Reset (if enabled – see RESL), GATE (if enabled – see GATE), Preset Counts (see PREC), Preset Time (see PRET), Preset Real Time (see PRER), the 'MCA Enable' and 'MCA Disable' Request Packets, and briefly during internal buffer operations.]

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified.

Example: GPME=ON; // Enable/disable the G.P. Counter with the MCA

5.1.25 HVSE - Turn On/Off the PX5/PC5 High Voltage Supply

Command: HVSE
Parameter: [{+|-}####|OFF]
Units: V
Default: OFF
Range: 0 to 1500V (for a positive HV PC5);
0 to -1500V (for a negative HV PC5);
-1500V to 1500V [PX5]
-5000V to 5000V [PX5 with HPGe HVPS option]

Dependencies: none
Supported: FW6.00 and later

Description: HVSE turns on or off the PC5 HV supply and sets the HV. The PC5 can have either a positive or negative supplies. The DP5 will compare the polarity of the parameter to the polarity of the PC5 HV supply, and will only turn on the HV supply if the specified polarity matches the PC5. [PX5 compares the polarity of the parameter to the position of the HV polarity jumper.]

Errors: DP5: An INVALID PARAMETER error will be returned if the PC5 does not have the same polarity HV supply as the voltage specified, or if the specified HV is outside the range listed. A PC5 NOT PRESENT error will be returned if a PC5 is not detected.
PX5: An INVALID PARAMETER error will be returned if the polarity of the specified voltage does not agree with the PX5 HV polarity jumper, or if the specified HV is outside the range listed.

Example:
```
HVSE=150;          // Set the PC5 HV supply to 150V, but only
                   // if it's a +HV PC5
```

5.1.26 INOF - Set the Input Offset

[DP5/PX5 only]

Command: INOF
Parameter: [{+|-}####|AU{TO}|DE{F}]
Units: MV (millivolts)
Default: DEF
Range: -2047mV to +2047mV

Dependencies: AINP, if 'DEF' is used; INOG, if INOG=HIGH (see below)
Supported: FW6.00 and later; not supported on DP5G, which does not have a variable input offset
Related: AINP, INOG

Description: INOF sets a DAC, which shifts the input to the ADC so that the signal is in the proper range. Generally, the default setting ('DEF') can be used, because a standard DP5 has an AC-coupled signal input which removes DC levels from the preamp. For a customized DP5 (or a PX5 with preamp pole cancellation enabled via 'PAPZ'), it may be necessary to set the input offset manually. If so, it should be set to produce a DC level of ~200mV (for AINP=NEG) or ~1.8V (for AINP=POS) at the test point AMP3OUT (DP5) or AMPOUT (PX5). [Note that in the DP5, there is a gain of 2 for the DAC output; changing INOF by 100mV results in the AMP3OUT testpoint shifting 200mV.]

In the PX5, the 'INOG' command can be used to change the gain of the input offset. If used, the 'INOG' command must precede INOF. If the high gain input offset ('INOG=HIGH') is used, then the 'DEF' (default) option for INOF cannot be used, and will result in an INVALID PARAMETER error.

The 'AUTO' parameter may be specified, in which case the DP5 or PX5 will search for an appropriate input offset. Note that the detector must be stable for this to work; if HV or temperature has not stabilized, then this will not operate properly.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of those listed.

Example: INOF=200; // Set the input offset DAC to 200mV

5.1.27 INOG - Set the Input Offset Gain

[PX5 only]

Command: INOG
Parameter: [LO{W}|HI{GH}]
Units: none
Default: LOW

Dependencies:
Supported: FW6.06 and later; PX5 only
Related: AINP, INOF

Description: In the PX5, the input offset is normally injected after the gain stages – this is the "LOW" setting. If preamp pole cancellation is used, then a DC offset may exist prior to the gain stages, and depending on gain, may result in an offset too large for the low gain input offset to correct. Selecting "HIGH" results in the input offset being injected earlier in the analog chain, so that it can correct a larger DC offset.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of those listed.

Example: INOG=HIGH; // Set the input offset gain to HIGH

5.1.28 LMMO – Select List-Mode operating mode

Command: LMMO
Parameter: [NO{RM}|DT{C}]
Units: none
Default: NORM

Dependencies: none
Supported: FW6.08.02 and later

Description: LMMO selects the List-Mode operating mode. LMMO=DTC enables the deadtime feature. In this mode, the 'tag' bit (see section 4.2.22) is used to identify events that have been rejected by PUR or RTD logic (if these are enabled.) These events are included in the List-Mode data so that they can be counted to extract a more accurate input count rate for deadtime calculation. In addition, detector reset events are also inserted in the data stream (identified by amplitude=0x0001), so that the deadtime calculation can include the time during which processing was disabled due to detector reset.

Errors: An INVALID PARAMETER error will be returned if the parameter is other than those listed, and NORM will be selected.

Example: LMMO=DTC; // Enable the List-mode deadtime feature

5.1.29 MCAC - Select Number of MCA Channels

Command: MCAC
Parameter: [256|512|1024|2048|4096|8192]
Units: channels
Default: 1024

Dependencies: none
Supported: FW6.00 and later

Description: MCAC selects the total number of channels for the MCA. [This is sometimes referred to as 'MCA Gain'.]

Errors: An INVALID PARAMETER error will be returned if the parameter is other than those listed, and 1024 channel operation will be selected.

Example: MCAC=512; // Select 512 MCA channels

5.1.30 MCAE - Initial State of MCA Enable

Command: MCAE
Parameter: [ON|OF{F}]
Units: none
Default: OFF

Dependencies: none
Supported: FW6.00 and later

Description: MCAE sets the initial state of MCA Enable. It determines whether the acquisition starts immediately after the Configuration Packet is processed ('ON'), or whether the DP5 will wait for an 'Enable MCA/MCS' Request Packet to start the acquisition ('OFF').

Errors: An INVALID PARAMETER error will be returned if the parameter is neither 'ON' nor 'OFF'.

Example: MCAE=ON; // Start taking data immediately

5.1.31 MCAS - Select the MCA Source

Command: MCAS
Parameter: [NO{RM}|MC{S}|FA{ST}| PU{R}|RT{D}]
Units: none
Default: NORM

Dependencies: RTDE
Supported: FW6.00 and later
Related:

Description: MCAS selects the operating mode of the MCA, as listed below:
'NORM' – normal MCA operation, using the shaped channel as the source

'MCS' - selects Multi-channel Scaler mode, rather than MCA. [MCS mode records counts vs. time, rather than counts vs. energy. MCSL and MCSH are used to set the MCA region that is counted in MCS mode.]

'FAST' – the MCA produces a spectrum using the Fast channel as the source, rather than the shaped channel. [This requires RTD to be disabled to work properly. See RTDE.]

'PUR' – the MCA records only piled-up events, rather than normal events. [This requires RTD to be disabled to work properly. See RTDE.]

'RTD' – the MCA records only events that would normally be rejected by RTD. [This requires RTD to be enabled to work properly. See RTDE, RTDS and RTDT.]

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of those listed, and 'NORM' will be used.

Example: MCAC=FAST; // Acquire a spectrum of the fast channel

5.1.32 MCSL - Set Low Threshold for MCS

Command: MCSL
Parameter: [####]
Units: channel
Default: 0
Range: Depends on number of channels specified by MCAC:
256 ch: 0 - 255
512 ch: 0 – 511
1024 ch: 0 - 1023
2048 ch: 0 - 2047
4096 ch: 0 - 4095
8192 ch: 0 – 8191

Dependencies: none
Supported: FW6.01 and later
Related: MCSH, MCST, MCAS

Description: MCSL sets the low threshold for the MCS (Multi-Channel Scaler). The low and high thresholds are exclusive; for example, PRCL=100 and PRCH=102 will only count events that occur in MCA channel 101. [The MCS thresholds only have meaning when the MCS operational mode is selected by the MCAS command.]

Errors: An INVALID PARAMETER error will be returned if the parameter is outside the range 0- 8191; it is not error-checked with regard to the ranges listed. If MCSL is set higher than MCSH, no error is generated, but no events will be counted as this is an impossible condition.

Example:
```
MCSL=100;        // Set MCS to count events from
MCSH=200;        //  channel 101 to 199
```

5.1.33 MCSH - Set High Threshold for MCS

Command: MCSH
Parameter: [####]
Units: channel
Default: 8191
Range: Depends on number of channels specified by MCAC:
256 ch: 0 - 255
512 ch: 0 – 511
1024 ch: 0 - 1023
2048 ch: 0 - 2047
4096 ch: 0 - 4095
8192 ch: 0 – 8191

Dependencies: none
Supported: FW6.01 and later
Related: MCSL, MCST, MCAS

Description: MCSH sets the high threshold for the MCS (Multi-Channel Scaler). The low and high thresholds are exclusive; for example, MCSL=100 and MCSH=102 will only count events that occur in MCA channel 101. [The MCS thresholds only have meaning when the MCS operational mode is selected by the MCAS command.]

Errors: An INVALID PARAMETER error will be returned if the parameter is outside the range 0- 8191; it is not error-checked with regard to the ranges listed. If MCSL is set higher than MCSH, no error is generated, but no events will be output or counted as this is an impossible condition.

Example:
```
MCSL=100;        // Set MCS to count events from
MCSH=200;        //  channel 101 to 199
```

5.1.34 MCST - Set the MCS Timebase

Command: MCST
Parameter: [###.###]
Units: S (seconds)
Default: 0
Range: 0 – 655.35s; 10mS precision

Dependencies: none
Supported: FW6.00 and later
Related: MCAS

Description: MCST configures the timebase used by the MCS (Multi-Channel Scaler) – this is the duration of each 'channel' in the MCS acquisition. It is only relevant if the acquisition is in MCS mode, rather than MCA mode. (See the MCAS command.)

Errors: An INVALID PARAMETER error will be returned if the parameter is not within the range specified.

Example: MCST=10; // Set the MCS timebase to 10 seconds per channel

5.1.35 PAPS - Turn On/Off the Preamp Power Supplies

[DP5/PX5 only]

Command: PAPS
Parameter: [8{.5}|5|OF{F}|ON] [DP5]
[8{.5}|5|OF{F}] [PX5]
[OF{F}|ON] [PX5 with HPGe HVPS option]
Units: V
Default: OFF

Dependencies: none
Supported: FW6.00 and later; not supported on DP5G

Description: PAPS turns on or off the PC5 preamp power supplies. The PC5 can have either +/-5V or +/-8.5V preamp supplies. If the 5 or 8.5 option is specified, the PC5 will be checked to verify if it's the commanded type before it is switched on. If 'ON' is commanded, this test will not be performed – the PC5 preamp supplies will be turned on regardless of which voltage they are. ['ON' is not an option for the PX5 – the voltage must be specified, except for a PX5 with the HPGe HVPS option – then only 'ON' and 'OFF' are accepted.]

Errors: An INVALID PARAMETER error will be returned if the PC5 does not have the preamp power supplies of the voltage specified, or if a parameter other than those listed is specified. A PC5 NOT PRESENT error will be returned if a PC5 is not detected.

Example:
```
PAPS=5;          // Turn on the PC5 preamp supplies, but only
                 // if it's a 5V PC5
```

5.1.36 PAPZ – Preamp Pole-Zero Cancellation

[Standard PX5 only, not HPGe version]

Command: PAPZ
Parameter: [####.#|OF{F}]
Units: US (microseconds)
Default: OFF
Range: 34.5-4387uS [firmware rounds to nearest of 127 discrete values; discrete values are 4386.7uS/n, for n=1…127]

Dependencies: none
Supported: FW6.05 and later; PX5 only

Description: PAPZ enables or disables the pole-zero cancellation in the PX5 front-end electronics, and selects the time constant to cancel. The specified time constant is rounded to the nearest discrete value. The equation to generate the discrete values is given in the 'Range' above. These values have a tolerance of roughly 1%. The 127 possible values, in uS, are:

34.5	39.5	46.2	55.5	69.6	93.3	141.5	292.4
34.8	39.9	46.7	56.2	70.8	95.4	146.2	313.3
35.1	40.2	47.2	57.0	71.9	97.5	151.3	337.4
35.4	40.6	47.7	57.7	73.1	99.7	156.7	365.6
35.7	41.0	48.2	58.5	74.4	102.0	162.5	398.8
36.0	41.4	48.7	59.3	75.6	104.4	168.7	438.7
36.3	41.8	49.3	60.1	77.0	107.0	175.5	487.4
36.6	42.2	49.8	60.9	78.3	109.7	182.8	548.3
36.9	42.6	50.4	61.8	79.8	112.5	190.7	626.7
37.2	43.0	51.0	62.7	81.2	115.4	199.4	731.1
37.5	43.4	51.6	63.6	82.8	118.6	208.9	877.3
37.8	43.9	52.2	64.5	84.4	121.9	219.3	1096.7
38.1	44.3	52.9	65.5	86.0	125.3	230.9	1462.2
38.5	44.8	53.5	66.5	87.7	129.0	243.7	2193.4
38.8	45.2	54.2	67.5	89.5	132.9	258.0	4386.7
39.2	45.7	54.8	68.5	91.4	137.1	274.2	

Errors: Parameter values between 34.5uS and 8773uS are rounded to the nearest discrete value from the table above. Outside that range, an INVALID PARAMETER error will be returned, and the pole-zero cancellation circuit will be switched off.

Example:
```
PAPZ=50;        // Turn on the pole-zero cancellation, and
                //  cancel a 50uS time constant
```

5.1.37 PAPZ – Preamp Pole-Zero Cancellation

[HPGe PX5 only, not standard version]

Command: PAPZ
Parameter: [####.#|OF{F}]
Units: US (microseconds)
Default: OFF
Range: 34.5-103.5uS [firmware rounds to nearest of 255 discrete values; discrete values are 13248uS/(n+128), for n=0…255]

Dependencies: none
Supported: FW6.07.01 and later; HPGe PX5 only [Status byte 42, bits D3:D0=0001 indicates presence of HPGe option]

Description: PAPZ enables or disables the pole-zero cancellation in the PX5 front-end electronics, and selects the time constant to cancel. The specified time constant is rounded to the nearest discrete value. The equation to generate the discrete values is given in the 'Range' above. These values have a tolerance of roughly 1%. The 255 possible values, in uS, are:

34.59	36.10	37.74	39.54	41.53	43.72	46.16	48.88	51.95	55.43	59.41	64.00	69.36	75.70	83.32	92.64
34.68	36.20	37.85	39.66	41.66	43.87	46.32	49.06	52.16	55.66	59.67	64.31	69.72	76.13	83.84	93.29
34.77	36.29	37.96	39.78	41.79	44.01	46.48	49.25	52.36	55.90	59.94	64.62	70.09	76.57	84.38	93.95
34.86	36.39	38.07	39.90	41.92	44.16	46.65	49.43	52.57	56.13	60.22	64.94	70.46	77.02	84.92	94.62
34.95	36.49	38.18	40.02	42.06	44.31	46.81	49.62	52.78	56.37	60.49	65.26	70.84	77.47	85.47	95.31
35.05	36.60	38.29	40.14	42.19	44.45	46.98	49.80	52.99	56.61	60.77	65.58	71.22	77.93	86.02	96.00
35.14	36.70	38.40	40.27	42.32	44.60	47.14	49.99	53.20	56.86	61.05	65.91	71.61	78.39	86.58	96.70
35.23	36.80	38.51	40.39	42.46	44.75	47.31	50.18	53.42	57.10	61.33	66.24	72.00	78.85	87.15	97.41
35.33	36.90	38.62	40.51	42.60	44.91	47.48	50.37	53.63	57.35	61.62	66.57	72.39	79.33	87.73	98.13
35.42	37.00	38.74	40.64	42.73	45.06	47.65	50.56	53.85	57.60	61.90	66.91	72.79	79.80	88.32	98.86
35.52	37.11	38.85	40.76	42.87	45.21	47.82	50.76	54.07	57.85	62.19	67.25	73.19	80.29	88.91	99.60
35.61	37.21	38.96	40.89	43.01	45.37	48.00	50.95	54.29	58.10	62.49	67.59	73.60	80.78	89.51	100.4
35.71	37.32	39.08	41.01	43.15	45.52	48.17	51.15	54.52	58.36	62.78	67.94	74.01	81.27	90.12	101.1
35.80	37.42	39.19	41.14	43.29	45.68	48.35	51.35	54.74	58.62	63.08	68.29	74.42	81.77	90.74	101.9
35.90	37.53	39.31	41.27	43.43	45.84	48.53	51.55	54.97	58.88	63.38	68.64	74.84	82.28	91.36	102.7
36.00	37.63	39.43	41.40	43.58	46.00	48.70	51.75	55.20	59.14	63.69	69.00	75.27	82.80	92.00	103.5

As of FW6.08.06, when PAPZ is enabled, the RESL command can be used to lockout processing after a saturating overrange event (these events can cause artifacts in the spectrum.) See Section 5.1.49.

Errors: Parameter values between 34.5uS and 103.5uS are rounded to the nearest discrete value from the table above. Outside that range, an INVALID PARAMETER error will be returned, and the pole-zero cancellation circuit will be switched off.

Example:
```
PAPZ=50;        // Turn on the pole-zero cancellation, and
                //  cancel a 50uS time constant
```

5.1.38 PDMD - Select the Peak Detect Mode [DP5, PX5, DP5G]

Command: PDMD
Parameter: [NO{RM}|MI{N}]
Units: none
Default: NORM

Dependencies: none
Supported: FW6.00 and later
Related: SOFF

Description: Normally, the DP5 Peak Detect unit searches for maxima in the shaped pulse stream, to determine which events to include in the spectrum. (This is the normal Peak Detect Mode; PDMD=NORM). PDMD=MIN configures the Peak Detect unit to search for both minima and maxima, in order for the MCA to be able to capture the 'noise Gaussian' around the zero energy point of the spectrum. Because the MCA can't capture negative peaks, the Spectrum Offset (SOFF) should be used to shift the spectrum positive, so the entire noise Gaussian can be captured.

Errors: An INVALID PARAMETER error will be returned if the parameter is not NORM or MIN.

Example: PDMD=MIN; // Set the Peak Detect to MIN+MAX mode

5.1.39 PDMD - Select the Peak Detect Mode [MCA8000D]

Command: PDMD
Parameter: [NO{RM}|MI{N}|AB{S}|CL{K}|IN{T}]
Units: none
Default: NORM

Dependencies: none
Supported: FW6.00 and later
Related: SOFF

Description: Normally, the DP5 Peak Detect unit searches for maxima in the shaped pulse stream, to determine which events to include in the spectrum. (This is the normal Peak Detect Mode; PDMD=NORM). PDMD=MIN configures the Peak Detect unit to search for both minima and maxima, in order for the MCA to be able to capture the 'noise Gaussian' around the zero energy point of the spectrum. Because the MCA can't capture negative peaks, the Spectrum Offset (SOFF) should be used to shift the spectrum positive, so the entire noise Gaussian can be captured.

ABS: Absolute peak mode – the single peak with the greatest amplitude is recorded for the interval from when the signal rises above the threshold to when it falls below the threshold.

CLK: Clocked mode – rather than detecting a peak, the instantaneous signal value is captured on the rising edge of an external clock connected to the GATE-2 input, and this value is used as the channel number for which the count is incremented in the histogram.

INT: Internal clock mode - rather than detecting a peak, the instantaneous signal value is captured on the rising edge of an internal clock which runs at 1.563MHz, and this value is used as the channel number for which the count is incremented in the histogram.

Errors: An INVALID PARAMETER error will be returned if the parameter is not NORM or MIN.

Example: PDMD=MIN; // Set the Peak Detect to MIN+MAX mode

5.1.40 PRCL - Set Low Threshold for Preset Counts

Command: PRCL
Parameter: [####]
Units: channel
Default: 0
Range: Depends on number of channels specified by MCAC:
256 ch: 0 - 255
512 ch: 0 – 511
1024 ch: 0 - 1023
2048 ch: 0 - 2047
4096 ch: 0 - 4095
8192 ch: 0 – 8191

Dependencies: none
Supported: FW6.01 and later
Related: PRCH, PREC

Description: PRCL sets the low threshold for the Preset Counts. The low and high thresholds are exclusive; for example, PRCL=100 and PRCH=102 will only count events that occur in channel 101.

Errors: An INVALID PARAMETER error will be returned if the parameter is outside the range 0- 8191; it is not error-checked with regard to the ranges listed. If PRCL is set higher than PRCH, no error is generated, but no events will be counted as this is an impossible condition.

Example:
```
PRCL=100;        // Set Preset Counts to count events from
PRCH=200;        //  channel 101 to 199
```

5.1.41 PRCH - Set High Threshold for Preset Counts

Command: PRCH
Parameter: [####]
Units: channel
Default: 8191
Range: Depends on number of channels specified by MCAC:
256 ch: 0 - 255
512 ch: 0 – 511
1024 ch: 0 - 1023
2048 ch: 0 - 2047
4096 ch: 0 - 4095
8192 ch: 0 – 8191

Dependencies: none
Supported: FW6.01 and later
Related: PRCL, PREC

Description: PRCH sets the high threshold for the Preset Counts. The low and high thresholds are exclusive; for example, PRCL=100 and PRCH=102 will only count events that occur in channel 101.

Errors: An INVALID PARAMETER error will be returned if the parameter is outside the range 0- 8191; it is not error-checked with regard to the ranges listed. If PRCL is set higher than PRCH, no error is generated, but no events will be output or counted as this is an impossible condition.

Example:
```
PRCL=100;        // Set Preset Counts to count events from
PRCH=200;        //  channel 101 to 199
```

5.1.42 PREC - Preset Counts

Command: PREC
Parameter: [##########|OF{F}]
Units: counts
Default: OFF
Range: 0 – 4,294,967,295 (i.e. 2^32 -1)

Dependencies: none
Supported: FW6.00 and later
Related: PRET, PRER, PRCL, PRCH

Description: PREC specifies the preset counts. The acquisition will stop automatically when the number of events registered between the channels specified by PRCL and PRCH reaches this value. If OFF (or 0) is specified, the acquisition will continue unless stopped by other means (PRET, PRER, MCA disable Request Packet, etc.) By configuring PREL and PREH appropriately, this command allows an acquisition to be stopped by the counts in a single channel, a ROI, or the entire spectrum.

Errors: No errors are returned – an unrecognized parameter is interpreted as 'OFF'. A number outside the range listed is converted to a 32-bit unsigned integer.

Example:
```
PREC=10000;     // Stop when the total counts between channels PRCL & PRCH
                //  reaches 10,000
```

5.1.43 PREL - Preset Livetime [MCA8000D only]

Command: PREL
Parameter: [########.###|OF{F}]
Units: S (seconds)
Default: OFF
Range: 0 – 4,294,967.29 seconds; 0.01 second precision
(Note that because the parameter field is limited to 10 characters, the following limit applies if 3 digits are required to the right of the decimal point)
0 – 999,999.999 seconds; 0.001 second precision

Dependencies: none
Supported: FW6.07.00 and later; MCA8000D only
Related: PREC, PRET, PRER

Description: PREL sets the preset livetime. The acquisition will stop automatically when the livetime reaches this value. If OFF (or 0) is specified, the acquisition will continue unless stopped by other means (PREC, PRET, MCA disable Request Packet, etc.)

Errors: An INVALID PARAMETER error will be returned if the parameter is not 'OFF' or a number within the range specified.

Example: PREL=100; // Stop the acquisition when livetime reaches 100s

5.1.44 PRER - Preset Real Time

Command: PRER
Parameter: [########.###|OF{F}]
Units: S (seconds)
Default: OFF
Range: 0 – 4,294,967.29 seconds; 0.01 second precision
(Note that because the parameter field is limited to 10 characters, the following limit applies if 3 digits are required to the right of the decimal point)
0 – 999,999.999 seconds; 0.001 second precision

Dependencies: none
Supported: FW6.01 and later
Related: PREC, PRET

Description: PRER sets the preset real time. The acquisition will stop automatically when the real time reaches this value. If OFF (or 0) is specified, the acquisition will continue unless stopped by other means (PREC, PRET, MCA disable Request Packet, etc.)

Errors: An INVALID PARAMETER error will be returned if the parameter is not 'OFF' or a number within the range specified.

Example: PRER=100; // Stop the acquisition when real time reaches 100s

5.1.45 PRET - Preset Acquisition Time

Command: PRET
Parameter: [########.#|OF{F}]
Units: S (seconds)
Default: OFF
Range: 0 – 99,999,999.9 seconds; 0.1 second precision

Dependencies: none
Supported: FW6.00 and later
Related: PREC, PRER

Description: PRET sets the preset acquisition time. The acquisition will stop automatically when the acquisition time reaches this value. If OFF (or 0) is specified, the acquisition will continue unless stopped by other means (PREC, PRER, MCA disable Request Packet, etc.)

Errors: An INVALID PARAMETER error will be returned if the parameter is not 'OFF' or a number within the range specified.

Example: PRET=100; // Stop the acquisition when it reaches 100s

5.1.46 PURE - Pile-up Reject Enable [DP5, PX5, DP5G, TB-5]

Command: PURE
Parameter: [ON|OF{F}|MA{X}|###.###]
Units: US (microseconds)
Default: OFF
Range: The table below specifies the range of the PUR interval as a function of peaking time and FPGA clock.

Dependencies: TPEA must precede PURE, if ###.### is specified. None, otherwise.
Supported: FW6.00 and later
Related: THFA

Description: PURE is used to enable or disable Pile-up Rejection. Normally (for PURE=ON), the Pile-up interval is dynamic; the DP5 varies the interval on a pulse-by-pulse basis to minimize deadtime. However, this can be overridden. The interval can be set to a constant, or to the maximum available. See the table below for allowable values. The PUR interval is started when a peak is detected on the Fast Channel which exceeds its threshold, so THFA must be set properly.

Errors: An INVALID PARAMETER error will be returned if the parameter is not ON, OFF, MAX, or within the range specified below. If a number is specified that is greater than is allowed, INVALID PARAMETER will be returned and the PUR interval will be set to its maximum.

Example: PURE=ON; // Enable Pile-up Rejection

FPGA Clock=20MHz			FPGA Clock=80MHz		
Peaking Time	**PUR Interval**	**Precision**	**Peaking Time**	**PUR Interval**	**Precision**
0.800 - 6.40uS	0 - 25.6uS	50nS	0.200 - 1.600uS	0 - 6.39uS	12.5nS
6.60 - 12.80uS	0 - 51.1uS	100nS	1.650 - 3.200uS	0 - 12.8uS	25nS
13.20 - 25.60uS	0 - 102.2uS	200nS	3.30 - 6.40uS	0 - 25.6uS	50nS
26.40 - 51.20uS	0 - 204.4uS	400nS	6.60 - 12.80uS	0 - 51.1uS	100nS
52.80 - 102.4uS	0 - 408.8uS	800nS	13.20 - 25.60uS	0 - 102.2uS	200nS

5.1.47 PURE - Pile-up Reject Enable [MCA8000D]

Command: PURE
Parameter: [HI{GH}| LO{W}|OF{F}]
Units: none
Default: OFF

Dependencies: none
Supported: FW6.00 and later

Description: PURE is used to enable or disable Pile-up Rejection, and to select whether the external signal is active high or active low. **The GATE2 input is used for Pile-up reject.** If 'HIGH' is selected, then events are accepted if the GATE2 input is high at the pulse peak, and rejected if the input is low. If 'LOW' is selected, then events are accepted if the GATE2 input is low at the pulse peak, and rejected if the input is high.

Errors: An INVALID PARAMETER error will be returned if the parameter is not HIGH, LOW or OFF.

Example: PURE=HI; // Enable Pile-up Rejection for an active-high input signal.

5.1.48 RESC - Reset the Configuration to Defaults

Command: RESC
Parameter: [Y]
Units: none
Default: none

Dependencies: none
Supported: FW6.00 and later
Related:

Description: RESC is used to reset the DP5's configuration to default settings. It resets each setting to the default listed for each command and in table XX. If it is used, it should be the first command in the ACII configuration packet.

RESC is useful because the DP5 stores the settings from previous configuration commands in non-volatile memory, and new

Errors: No error is returned regardless of the parameter, but the configuration is only reset if the parameter is 'Y'.

Example: RESC=Y; // Reset the configuration to default settings

5.1.49 RESL - Select Reset Lockout Interval

Command: RESL
Parameter: [#####|OF{F}]
Units: US (microseconds)
Range: **FW6.07.03 and earlier:** The DP5 will select the nearest available Reset Lockout Interval from the following list:

FPGA clock=80MHz: 25.6uS, 51.2uS, 102.4uS, 204.8uS, 409.6uS, 819.2uS, 1638.4uS, 3276.8uS

FPGA clock=20MHz: 102.4uS, 204.8uS, 409.6uS, 819.2uS, 1638.4uS, 3276.8uS, 6553.6uS, 13107.2uS

FW6.07.04 and later: The reset lockout interval can be set with 1uS precision, over the range of 1uS to 3226uS.

FW6.08.03/FP6.09 and later: The DPG/Gammarad/TB5 can use this to lockout processing after a cosmic ray event. A cosmic ray may produce a very large response with a significant tail, which can cause spurious events to be recorded. Using RESL with a sufficiently long interval may eliminate these events.

FW6.08.06/FP6.11 and later: The PX5 HPGe can use this to lockout processing after a cosmic ray event. A cosmic ray may produce a very large response with a significant tail, which can cause spurious events to be recorded. Using RESL with a sufficiently long interval may eliminate these events. This function is enabled only when PAPZ (Preamp Pole-Zero cancellation) is enabled.

Default: OFF

Dependencies: TPEA must precede RESL
Supported: FW6.00 and later
Related:

Description: RESL determines whether the MCA data taking will be paused when a detector reset is detected. If OFF is selected, then the detection of detector reset is disabled. Otherwise, the nearest value from those listed in *Range* will be selected.

Errors: No error checking is done on the parameter; the next largest value in *Range* will be used if a number is specified. If the parameter isn't recognized, the lowest value in *Range* is used.

Example:
```
RESL=1000;  // This selects a Reset Lockout Interval of 1638.4uS
            //  or 1000uS in FW6.07.04 and later
```

5.1.50 RTDD - Set Custom RTD Oneshot Delay

Command: RTDD
Parameter: [###]
Units: decimated clocks
Default: none
Range: 1 - 127

Dependencies: RTDE must precede RTDD
Supported: FW6.00 and later
Related: RTDE, RTDS, RTDT, RTDW

Description: RTDD is used to fine-tune the timing of the RTD logic. It may be needed for events with very slow risetimes, or configurations where the shaper produces a non-trapezoidal/cusp shape. For these events, the peak of the shaped event may not occur when it is expected. The standard RTD timing parameters are calculated when the RTDE command is received, so the RTDW & RTDD commands must come after RTDE, so that they can override the standard timing.

To fine-tune the RTD timing:

1. Use DACO=SHAPED and AUO2=5 (for RTD_ONESHOT). Use an oscilloscope to view both signals. Trigger on either.

2. Use the parameters for RTDW and RTDD to adjust the width and delay of the RTD_ONESHOT signal – it should bracket the time during which the peak occurs for a variety of pulses.

Errors: An INVALID PARAMETER error will be returned if the parameter is not in the *range* specified.

Example:
```
RTDD=60;        // Override the standard RTD timing – set the
                // RTD Oneshot delay to 60 decimated clocks
```

5.1.51 RTDE - Enable Risetime Discrimination

Command: RTDE
Parameter: [ON|OF{F}]
Units: none
Default: OFF

Dependencies: TPEA & TFLA
Supported: FW6.00 and later
Related: RTDT, RTDS

Description: RTDE is used to enable risetime discrimination (RTD). RTDS and RTDT are also needed to completely configure RTD. For very slow or distorted pulses, RTDW and RTDD may be needed, to override standard RTD timing parameters.

Errors: An INVALID PARAMETER error will be returned if the parameter is not ON or OFF, and RTD will be disabled.

Example: RTDE=ON; // Enable Pile-up Rejection

5.1.52 RTDS - Set Risetime Discrimination Sensitivity

Command: RTDS
Parameter: [####]
Units: %
Default: 0%
Range: 2-398% (1.5% precision), 400-1593% (6.5% precision) [FW6.08.05 and earlier]
2-398% (1.5% precision), 400-3187% (13% precision) [FW6.08.06 and later]

Dependencies: none
Supported: FW6.00 and later
Related: RTDE, RTDT

Description: RTDS sets the Risetime Discrimination (RTD) Sensitivity. RTD is performed by taking the ratio of the peak slow channel amplitude to the peak fast channel amplitude for a given pulse – the event is rejected if the ratio is above the sensitivity setting. [As the risetime gets slower, the fast channel response falls off faster than the slow channel, so the ratio increases for the event.] If the peak slow channel amplitude is below the RTD Threshold (see RTDT), it will be accepted regardless of the ratio and sensitivity settings. This command has no effect if RTD is disabled (see RTDE).

Errors: An INVALID PARAMETER error will be returned if the parameter is not within the range specified, and the sensitivity will be set to 0%.

Example: RTDS=500; // Set the RTD Sensitivity to 500%

5.1.53 RTDT - Set Risetime Discrimination Threshold

Command: RTDT
Parameter: [##.###]
Units: % full-scale
Default: 0%
Range: 0-49.9% (~0.2% precision)

Dependencies: none
Supported: FW6.00 and later
Related: RTDE, RTDS

Description: RTDT sets the Risetime Discrimination (RTD) Threshold. If the peak slow channel amplitude is below the RTD Threshold, it will be accepted regardless of the sensitivity setting. This has no effect if RTD is disabled (see RTDE).

Errors: An INVALID PARAMETER error will be returned if the parameter is not within the range specified, and the threshold will be set to 49.9% (or 0% if a negative number is specified).

Example:
```
RTDT=10;        // Set the RTD Threshold to 10% full-scale.
                // i.e. for 1K channels, 10% = channel 102
```

5.1.54 RTDW - Set Custom RTD Oneshot Width

Command: RTDW
Parameter: [###]
Units: decimated clocks
Default: none
Range: 1 - 127

Dependencies: RTDE must precede RTDW
Supported: FW6.00 and later
Related: RTDE, RTDS, RTDT, RTDD

Description: RTDW is used to fine-tune the timing of the RTD logic. It may be needed for events with very slow risetimes, or configurations where the shaper produces a non-trapezoidal/cusp shape. For these events, the peak of the shaped event may not occur when it is expected. The standard RTD timing parameters are calculated when the RTDE command is received, so the RTDW & RTDD commands must come after RTDE, so that they can override the standard timing.

For instructions on how to fine-tune the RTD timing, see the 'RTDD' command.

Errors: An INVALID PARAMETER error will be returned if the parameter is not in the *range* specified.

Example:
```
RTDW=60;        // Override the standard RTD timing – set the
                // RTD Oneshot period to 60 decimated clocks
```

5.1.55 SCAH - Set SCA High Threshold

Command: SCAH
Parameter: [####]
Units: channel
Default: 8191 (for all SCAs)
Range: Depends on number of channels specified by MCAC:
256 ch: 0 - 255
512 ch: 0 – 511
1024 ch: 0 - 1023
2048 ch: 0 - 2047
4096 ch: 0 - 4095
8192 ch: 0 – 8191

Dependencies: SCAI must precede SCAH
Supported: FW6.00 and later
Related: SCAI, SCAL, SCAO; SCAW is not indexed

Description: SCAH sets the high threshold for the SCA referenced by the SCA Index (SCAI). The low and high thresholds are exclusive; for example, SCAL=100 and SCAH=102 will only output events that occur in channel 101.

Errors: An INVALID PARAMETER error will be returned if the parameter is outside the range 0- 8191; it is not error-checked with regard to the ranges listed. If SCAL is set higher than SCAH, no error is generated, but no events will be output or counted as this is an impossible condition.

Example:
```
SCAI=2;          // Set the SCA Index to 2; enable SCA2 output as
                 // active high
SCAL=100;        // Set the SCA2 LLD to channel 100
SCAH=200;        // Set the SCA2 HLD to channel 200
```

5.1.56 SCAI - Set SCA Index

Command: SCAI
Parameter: [#]
Units: none
Default: none
Range: 1-16

Dependencies:
Supported: FW6.00 and later
Related: SCAL, SCAH, SCAO; SCAW is not indexed

Description: SCAI is used in conjunction with the SCAL, SCAH and SCAO commands to specify which SCA these commands will apply to. When the SCA index is set to 1 through 8, it also enables the specified SCA output and sets it to active high, so the SCAO command doesn't need to be specified unless a different output option is needed.

Errors: An INVALID PARAMETER error will be returned if the parameter is not within the range specified.

Example:
```
SCAI=2;          // Set the SCA Index to 2; enable SCA2 output as
                 // active high
SCAL=100;        // Set the SCA2 LLD to channel 100
SCAH=200;        // Set the SCA2 HLD to channel 200
```

5.1.57 SCAL - Set SCA Low Threshold

Command: SCAL
Parameter: [####]
Units: channel
Default: 0 (for all SCAs)
Range: Depends on number of channels specified by MCAC:
256 ch: 0 - 255
512 ch: 0 – 511
1024 ch: 0 - 1023
2048 ch: 0 - 2047
4096 ch: 0 - 4095
8192 ch: 0 – 8191

Dependencies: SCAI must precede SCAL
Supported: FW6.00 and later
Related: SCAI, SCAH, SCAO; SCAW is not indexed

Description: SCAL sets the low threshold for the SCA referenced by the SCA Index (SCAI). The low and high thresholds are exclusive; for example, SCAL=100 and SCAH=102 will only output events that occur in channel 101.

Errors: An INVALID PARAMETER error will be returned if the parameter is outside the range 0- 8191; it is not error-checked with regard to the ranges listed. If SCAL is set higher than SCAH, no error is generated, but no events will be output or counted as this is an impossible condition.

Example:
```
SCAI=2;          // Set the SCA Index to 2; enable SCA2 output as
                 // active high
SCAL=100;        // Set the SCA2 LLD to channel 100
SCAH=200;        // Set the SCA2 HLD to channel 200
```

5.1.58 SCAO - Select SCA Output Level

Command: SCAO
Parameter: [OF{F}|HI{GH}|LO{W}]
Units: none
Default: OFF; HIGH when SCAI is set for an SCA

Dependencies: SCAI must precede SCAO
Supported: FW6.00 and later
Related: SCAI, SCAL, SCAH; SCAW is not indexed

Description: SCAO configures the output of the indexed SCA. For a setting of 'OFF', the indexed SCA output will always be low. For a setting of 'HIGH', the indexed output will be normally low and will produce a high pulse when an event occurs between the SCA low and high thresholds. For a setting of 'LOW', the indexed output will be normally high and will produce a low pulse. Note: only SCAs 1-8 have pulse outputs; SCAs 9-16 have counters, not pulse outputs. Also, if the SCA outputs 1-8 are all OFF, then the outputs are all tri-stated. If any of the outputs 1-8 are enabled, then they all are driven.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of those specified in *range*. Selecting the output level when the SCA index is set to 9-16 has no meaning, since these SCAs don't have outputs, but this will not produce an error.

Example:
```
SCAI=2;          // Set the SCA Index to 2; enable SCA2 output as
                 // active high
SCAO=LOW;        // Set SCA2 to an active low output instead
```

5.1.59 SCAW - Select SCA Output Pulse Width

Command: SCAW
Parameter: [100|1000]
Units: NS (nanoseconds)
Default: 100

Dependencies: none
Supported: FW6.00 and later
Related: SCAI, SCAL, SCAH

Description: SCAW sets the output pulse width for SCA 1-8. (SCA 9-16 don't have outputs.) This setting isn't indexed like other SCA settings; it applies to all 8 SCAs.

Errors: An INVALID PARAMETER error will be returned if the parameter is not 100 or 1000, and the width will be set to 100.

Example: SCAW=1000; // Set SCA 1-8 to produce 1000nS pulses

5.1.60 SCOE - Set Digital Scope Trigger Edge

Command: SCOE
Parameter: [RI{SING}|FA{LLING}]
Units: none
Default: RISING

Dependencies: none
Supported: FW6.00 and later
Related: SCOT, SCOG, AUO1, DACO; 'Arm Digital Scope' Request Packet

Description: SCOE sets the trigger edge polarity of the internal digital oscilloscope. (Note: The internal scope uses the selected AUX_OUT1 signal as the trigger source. The scope captures 2048 samples of the signal selected by DACO. Also, the scope must be armed before a trigger can occur. See 'Arm Digital Scope' Request Packet.)

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified.

Example:
```
SCOE=RISING;      // Trigger the internal scope on the rising edge of
                  // of the trigger (selected AUX_OUT1 signal)
```

5.1.61 SCOG - Set Digital Scope Gain

Command: SCOG
Parameter: [1|4|16]
Units: none
Default: 1

Dependencies: none
Supported: FW6.00 and later
Related: SCOE, SCOT, AUO1, DACO; 'Arm Digital Scope' Request Packet

Description: SCOG sets the gain of the internal digital oscilloscope. (SCOG does not affect the DAC output.) The signal is not clamped for gains of 4 or 16; it will roll over, so care must be taken to interpret the results accordingly. (Note: The internal scope uses the selected AUX_OUT1 signal as the trigger source. The scope captures 2048 samples of the signal selected by DACO. Also, the scope must be armed before a trigger can occur. See 'Arm Digital Scope' Request Packet.)

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified.

Example: SCOG=4; // Set the scope gain to 4x

5.1.62 SCOT - Set Digital Scope Trigger Position

Command: SCOT
Parameter: [87|50|12|-25]
Units: %
Default: 87%

Dependencies: none
Supported: FW6.00 and later
Related: SCOE, SCOG, AUO1, DACO; 'Arm Digital Scope' Request Packet

Description: SCOT sets the trigger position of the internal digital oscilloscope. 12%, 50% or 87% means that the trigger will be positioned at the 12%, 50% or 87% point of the digital scope data (i.e. the first 246, 1024 or 1782 samples are prior to the trigger and the rest are after the trigger.) -25% means that the trigger occurred 512 samples prior to the start of the scope data. (Note: The internal scope uses the selected AUX_OUT1 signal as the trigger source. The scope captures 2048 samples of the signal selected by DACO. Also, the scope must be armed before a trigger can occur. See 'Arm Digital Scope' Request Packet.)

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified.

Example: SCOT=12; // Set the trigger position to 12%

5.1.63 SCTC - Set Scintillator Time Constant

Command: SCTC
Parameter: [####|OF{F}]
Units: NS
Default: OFF
Range: 0-1599nS
Precision: 6.25nS @ 20MHz FPGA clock; 1.56nS @ 80MHz

Dependencies: TPEA must precede SCTC
Supported: FW6.08.01 and later; DP5G and TB-5 only

Description: SCTC sets the decay time constant of the scintillator material. The pulse processing logic uses this setting to attempt to cancel the effects of the time constant, to produce a more accurate trapezoidal shaped pulse. This setting may take some experimentation to find the appropriate setting; generally a setting equal to or a bit less than the actual scintillator time constant works best.

Errors: An INVALID PARAMETER error will be returned if the parameter is not in the range specified

Example: SCTC=230; // Set the scintillator time constant to 230nS (for NaI)

5.1.64 SOFF - Set Spectrum Offset

Command: SOFF
Parameter: [OF{F}|{+|-}####.###]
Units: channels
Default: OFF
Range: Depends on number of channels specified by MCAC:
256 ch: -256 to +255.992 ch; 1/128 ch precision
512 ch: -512 to +511.984 ch; 1/64 ch precision
1024 ch: -1024 to +1023.969 ch; 1/32 ch precision
2048 ch: -2048 to +2047.937 ch; 1/16 ch precision
4096 ch: -4096 to +4095.875 ch; 1/8 ch precision
8192 ch: -8192 to +8191.75 ch; 1/4 ch precision

Dependencies: MCAC must be sent prior to SOFF
Supported: FW6.00 and later
Related:

Description: SOFF can be used to specify the spectrum offset, if desired. Applying a positive offset will shift the spectrum up (i.e. higher in energy), while a negative offset shifts the spectrum down.

Errors: An INVALID PARAMETER error will be returned if the parameter is not within the range specified.

Example: SOFF=10.5; // Shift the spectrum up by 10.5 channels

5.1.65 SYNC – Select List-Mode Sync Source

Command: SYNC
Parameter: [IN{T}|EX{T}|FR{AME}|NO{TIMETAG}]
Units: none
Default: INT

Dependencies: none
Supported: FW6.06.05 and later
Related: CLKL

Description: SYNC selects the sync source for List-mode:

INT: Internal sync. The List-mode timer is reset to 0 by the 'Clear/Sync List-mode timer' request packet.

EXT: External sync. A rising edge on the input listed below will reset the List-mode timer to 0. The 'Clear/Sync List-mode timer' request packet also resets the timer. In this mode, the rollover of the least-significant 16 bits of the timer will trigger a Timetag record, as described in Section 4.2.22.

FRAME: External sync. A rising edge on the input listed below will reset the List-mode timer to 0, increment the Frame Count, and also trigger a Frame+Timetag record (as described in Section 4.2.22). The 'Clear/Sync List-mode timer' request packet resets both the timer and frame count to 0. In this mode, the rollover of the least-significant 16 bits of the timer will trigger a Frame+Timetag record.

NOTIMETAG: Internal sync. Same as 'INT', above, except each event is 16 bits, not 32 bits. There is no timetag stored with each event, only timer rollovers result in a timetag being stored in the data stream, at 100uS or 1mS rate. See Section 6.1.

The external sync signal should be connected to the following input:
PX5/Gammarad: The AUX-1 input. 'CON1=AUXIN1' must be commanded;
DP5: The AUXIN2 input.
DPG: The AUX1 input. 'CON1=AUXIN1' must be commanded.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of those listed.

Example: SYNC=EX; // Select external sync for List-mode

5.1.66 TECS - Turn On/Off the PC5 Thermoelectric Cooler (TEC) Supply and Set the Temperature

Command: TECS
Parameter: [###|OF{F}]
Units: K
Default: OFF
Range: 0-299K; ~0.1K precision

Dependencies: none
Supported: FW6.00 and later; not supported on DP5G

Description: TECS turns the PC5 TEC supply on or off, and sets the TEC temperature setpoint.

Errors: An INVALID PARAMETER error will be returned if the specified temperature is outside the range listed. A PC5 NOT PRESENT error will be returned if a PC5 is not detected.

Example: TECS=220K; // Turn on the TEC supply and cool to 220K
// or as cool as possible

5.1.67 TFLA - Select Flat Top Width

Command: TFLA
Parameter: [##.###]
Units: US (microseconds)
Range: The range is determined by the selected peaking time; see the table under the TPEA command.
Default: 0uS

Dependencies: TPEA must precede TFLA
Supported: FW6.00 and later
Related: TPEA

Description: TFLA selects the flat top width of the trapezoidal shaper. A flat top of 0uS will result in a triangular shape, not trapezoidal. The commanded peaking time (TPEA) determines the precision with which the flat top width can be commanded; the DP5 will round the commanded setting to the next lowest one.

Errors: An INVALID PARAMETER error will be returned if the commanded flat top is outside the range given in the TPEA table.

Example: TFLA=10; // This selects a flat top width of 10.00uS.

5.1.68 THFA - Select Threshold for Fast Channel

Command: THFA
Parameter: [###.##] {[###] in firmware prior to FW6.05}
Units: unitless
Range: 0-255.93 [256 equates to 50% of full-scale]
0-511.93 [FW6.07.05 and later; 512 equates to 100% of full-scale]
Precision: 1 part in 4096
1 part in 8192 [FW6.07.05 and later]
Default: 0

Dependencies: none
Supported: FW6.00 and later; range doubled in FW6.07.05 and later
Related: PURE

Description: THFA sets the threshold for the fast channel. [Generally, the ideal fast threshold is determined empirically, or by using the 'Autoset Fast Threshold' request packet (which only works in the absence of a source.) This is discussed in detail elsewhere.]

The units or scale factor is somewhat problematic, because the fast channel doesn't have a digital fine gain control like the shaped channel does, so only changes in coarse (analog) gain affect the fast channel. The 'MCAS' (MCA Source) command can be used to route the fast channel into the MCA, so that a spectrum of the fast channel can be inspected.

The parameter is a multiple of 1/16. It ranges from 0/16 to 4095/16 (or 8191/16). This awkward-seeming arrangement was done to increase the precision of the setting, while maintaining backward compatibility to custom software, configuration files, etc.

Errors: An INVALID PARAMETER error will be returned if the commanded threshold is outside the range given.

Example: THFA=10; // This sets the fast threshold to 10.

5.1.69 THSL - Select Threshold for Shaped Channel

Command: THSL
Parameter: [##.###]
Units: % (percent of full-scale)
Range: 0-24.9% (with approx. 0.1% precision; approx. 0.01% precision for FW6.06 and later)
Default: 0

Dependencies: none
Supported: FW6.00 and later
Related: THFA, TLLD

Description: THSL sets the noise threshold for the peak detect unit. Events below this threshold will not be recorded in the spectrum; this acts as a low-level discriminator (LLD). [Use the 'TLLD' command in addition to 'THSL' if it is desirable to have the LLD reject more than just noise.]

Errors: An INVALID PARAMETER error will be returned if the commanded threshold is outside the range given.

Example: THSL=4.5; // This sets the shaped threshold to 4.5% of full scale

5.1.70 TLLD - Select Threshold for Low-Level Discriminator (LLD)

Command: TLLD
Parameter: [####|OF{F}]
Units: channels
Range: 256 ch: 0 - 255
512 ch: 0 – 511
1024 ch: 0 - 1023
2048 ch: 0 - 2047
4096 ch: 0 - 4095
8192 ch: 0 – 8191

Default: OFF

Dependencies: none
Supported: FW6.01 and later
Related: THSL

Description: TLLD sets the low-level discriminator (LLD) for the MCA; only events above this channel will be recorded in the spectrum. If the LLD is enabled (i.e. not OFF), then events must be above both the LLD threshold and the shaped (slow) threshold (see THSL) to be recorded.

Errors: An INVALID PARAMETER error will be returned if the parameter is outside the range 0- 8191; it is not error-checked with regard to the ranges listed.

Example: TLLD=110; // Events in channels 110 or lower are rejected

5.1.71 TPEA - Set Peaking Time

Command: TPEA
Parameter: [###.###]
Units: US (microseconds)
Range: 0.8-102.4uS (CLK=20MHz), 0.05-25.6uS (CLK=80MHz), 0.05-102.4uS (CLK=AUTO)
Default: None – this command is required.

Dependencies: CLCK (if used) must precede TPEA
Supported: FW6.00 and later; FW6.02 and earlier don't support 80MHz peaking times slower than 0.200uS
Related: TFLA

Description: TPEA selects the peaking time for the slow (shaped) channel. If CLCK=AUTO (automatic CLK selection) is commanded prior to TPEA, then TPEA will set the FPGA clock to 80MHz for peaking times of less than 5uS, and 20MHz for peaking times of 5uS or greater. The precision with which the peaking time can be programmed is listed below. [The selected peaking time also determines the range and precision of available flat top widths, so those are listed as well.] The DP5 will round the commanded peaking time to the next lowest one, so an error will only be returned if the commanded peaking time is outside the range listed above.

Errors: An INVALID PARAMETER error will be returned if the commanded peaking time is outside the range given.

Example:
```
TPEA=10;    // This selects a peaking time of 10.00uS. If
            // CLCK=AUTO was commanded prior to this, then
            // the FPGA clock will be set to 20MHz
```

FPGA Clock=20MHz				FPGA Clock=80MHz			
Peaking Time	**Precision**	**Flat Top**	**Precision**	**Peaking Time**	**Precision**	**Flat Top**	**Precision**
0.800 - 6.40uS	100nS	0.05 – 3.15uS	50nS	0.050 - 1.600uS	25nS	12.5 – 787nS	12.5nS
6.60 - 12.80uS	200nS	0.1 – 6.30uS	100nS	1.650 - 3.200uS	50nS	25 – 1575nS	25nS
13.20 - 25.60uS	400nS	0.2 – 12.60uS	200nS	3.30 - 6.40uS	100nS	50 – 3150nS	50nS
26.40 - 51.20uS	800nS	0.4 – 25.2uS	400nS	6.60 - 12.80uS	200nS	0.1 – 6.30uS	100nS
52.80 - 102.4uS	1600nS	0.8 – 50.4uS	800nS	13.20 - 25.60uS	400nS	0.2 – 12.6uS	200nS

5.1.72 TPFA - Select Peaking Time for Fast Channel

Command: TPFA
Parameter: [50|100|200|400|1600]
Units: NS (nanoseconds)
Range: 50, 100, 200, 400 or 800nS for 80MHz FPGA clock; 200, 400, 800, 1600 or 3200nS for 20MHz FPGA clock.
Default: 100 for 80MHz clock; 400 for 20MHz clock

Dependencies: TPEA must precede TPFA
Supported: FW6.00 and later (50 & 200 settings require FW6.01 or later; 200 & 800 (80MHz) and 800 & 3200 (20MHz) require FW6.07.05 or later)
Related: THFA, TPFF

Description: TPFA selects the peaking time for the fast channel. There are five settings available for each FPGA clock rate; the 200, 400 and 800nS settings are available at both FPGA clock rates.

Errors: An INVALID PARAMETER error will be returned if the parameter violates the conditions listed under *Range*.

Example:
```
TPFA=400;   // This selects a fast channel peaking time of 400nS,
            // regardless of the FPGA clock.
```

5.1.73 TPMO - Select Test Pulser Mode

Command: TPMO
Parameter: [OF{F}|+S{NG}|+D{BL}| -S{NG}|-D{BL}]
Units: none
Default: OFF

Dependencies: none
Supported: FW6.00 and later
Related: DACF

Description: TPMO selects whether the Test Pulser is enabled, and if so, what type of pulses it produces. The test pulser uses the DAC output to simulate the output from a reset-style preamplifier. It produces a step in the DAC output at a rate of 2kHz. This signal is intended to be connected directly to the DP5 signal input for test and diagnostic purposes.

If +SNG or –SNG is specified, the DAC step is 1/4 of the value specified by the DACF command. (i.e. for DACF=200MV, "+SNG" produces +50mV steps and "-SNG" produces -50mV steps.) If +DBL or –DBL is specified, two step sizes are produced alternately; one is ¼ the value specified DACF, the other is 1/16 the value. (i.e. for DACF=200MV, "+DBL" produces +50mV and +12.5mV steps alternately; "-DBL" produces -50mV and -12.5mV steps alternately.)

For really large steps, a negative DACF can be used. This is treated as an unsigned value; to calculate the resulting step size from a negative DACF setting, use 1V+(DACF parameter). For example, for DACF=-200MV, +SNG produces ¼ (1V + -200mV) = 200mV steps.

Detector Reset Lockout (RESL) should be disabled or set to a short interval when the test pulser is enabled, since a detector reset is simulated when the DAC output wraps around. (It produces a large pulse of the polarity opposite the desired pulses, which looks like a detector reset.)

Note that if the Test Pulser is enabled, the internal digital scope will still capture the signal specified by DACO, even though the DAC will output test pulses.

Note: The PX5 has internal switches to connect the test pulser to the analog input. The DP5 does not; connect a test lead from J4 pin 1 to J8 pin 1 to use the test pulser.

Errors: An INVALID PARAMETER error will be returned if the parameter is not one of the values specified.

Example:
```
TPMO=+SNG;          // Enable the test pulser to produce single
                    // positive-going steps
```

5.1.74 VOLU – Turn the PX5 speaker ON/OFF

Command: VOLU
Parameter: [ON|OF{F}]
Range: ON or OF{F}
Default: OFF

Dependencies: none
Supported: FW6.01 and later; PX5 only, not supported by DP5 or DP5G, which don't have speakers

Description: This turns the PX5 speaker on or off. This simulates a Geiger counter, and produces a click for each event recorded by the fast channel.

Errors: An INVALID PARAMETER error will be returned if the parameter is not ON or OF{F}.

Example: VOLU=ON; // Enable the PX5 speaker

6 Select Topics

6.1 List-mode operation

List-mode refers to a data set that contains amplitude and timing information about each event, as opposed to a spectrum. When an event is detected by the DP5, if it passes all the acceptance criteria, then it is added into the spectrum. Its amplitude (channel number) and time are also recorded in the List-mode FIFO. Periodically, the List-mode timer least-significant bits roll over, and this triggers the writing of the most-significant bits of the timer into the FIFO. (This reduces the data requirements, by not writing the entire 47-bit time tag for every event.)

The count rate that List-mode can support is dependent on the interface used, and how fast the application is able to transfer data. Theoretically, the USB implementation can sustain roughly 150,000 counts per second, but this requires an application that can reliably perform data requests every 5mS, or perhaps faster. (The VB Demo uses a multimedia timer to request data every 5mS, and it is able to sustain about 100,000 counts per second. But it's easy to cause data dropouts due to the architecture of Visual Basic.)

There is also a 16-bit mode of operation. In this mode, no timetag is stored with each event, to further reduce the data requirement. The timetag is inserted into the datastream at either a 1kHz or 10kHz rate. This leads to a significant amount of data being generated at low count rates (32kbps/320kbps with no input counts), but it produces less at high count rates. This mode allows a maximum count rate of roughly 240,000 counts per second. Also, in the 16-bit mode, no events or timetags are recorded while MCA Enable is inactive, or GATE is enabled but de-asserted.

Ethernet can sustain around 12,000 counts per second. Ethernet is not well suited to List-mode because collisions can occur, causing retransmissions, which interfere with the periodic data transfer. (A quiet network is a necessity.)

RS232 can sustain around 2,000 counts per second at 115kbaud.

The List-mode timer is free-running, and cannot be stopped. It can be reset by sending a Request Packet to the DP5, or via a hardware signal.

List-mode data acquisition runs simultaneous to a spectrum acquisition. When the MCA is paused (via the 'MCA Enable' command, or briefly during spectrum readout), the List-mode data taking is also paused. (The List-mode timer continues to run.) Everything that qualifies whether an event is accepted into the spectrum also qualifies whether it is accepted into the List-mode buffer. This includes thresholds (slow and LLD), PUR, RTD, GATE, presets, and reset lockout, depending on how these are configured.

There are only two List-mode configuration options: CLKL (see section 5.1.12), and SYNC (see section 5.1.65). In normal List-mode operation, CLKL selects whether the List-mode timer operates at 1MHz (1uS per tick), or 10MHz (100nS per tick). In 16-bit mode (SYNC=NOTIMETAG), CLKL selects whether the timetags occur in the data stream at 10kHz (100uS) or 1kHz (1mS). SYNC selects whether an external signal is used to synchronize the List-mode timer, and, if so, also selects between two alternate data formats. SYNC is also used to select the 16-bit mode, in which case external sync is not available.

As of FW6.08.02, there is an additional command, which aids in deadtime calculation. LMMO (see section 5.1.28) allows piled-up events and detector resets to be included in the datastream (see section 4.2.22).

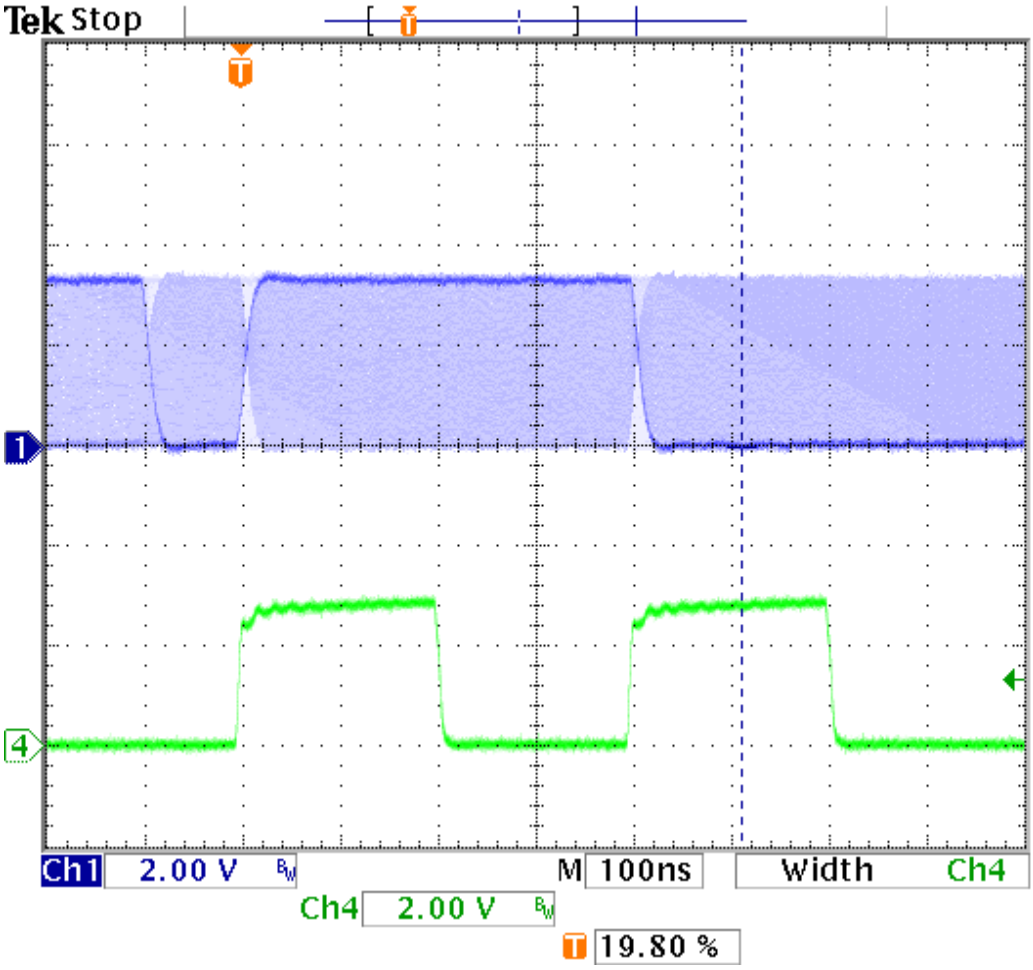
There are several request packets used for managing List-mode operation: 'Clear Spectrum' (see section 4.1.20) also clears the List-mode FIFO; and 'Clear/Sync List-mode timer' clears the List-mode timer, and triggers a timer rollover (see section 4.1.39).

The 'Request List-Mode Data' Request Packet (section 4.1.13) will result in a List-mode Data Response Packet (section 4.2.22) being sent. The List-mode Data Packet uses two different PIDs to indicate the state of the List-mode FIFO (full/not full). When the List-mode data packet indicates that the FIFO is full, that means that events were lost. When the FIFO is full, subsequent events are lost, rather than the initial ones. The FIFO is 4096 bytes in size, which means it can hold a combination of 1024 events and timetags. (Each record is 32 bits in size, as described in section.4.2.22.)

6.2 Streaming-mode operation

With the Streaming mode enabled, the SCA signals are reconfigured into an 8-bit bus, and the amplitude of each valid event is written out in two bytes. The AUX_OUT2 signal is used as a strobe; the data changes on the rising edge, and should be latched on the falling edge. SCA8 is an LSB/MSB indicator: when low, the remaining 7 bits (SCA7-1) are the least-significant bits of the 14-bit amplitude. When SCA8 is high, SCA7-1 are the most-significant bits of the 14-bit amplitude.

The oscilloscope capture below shows the relative timing of the signals. The trace on the bottom is the strobe, as output via CON2 (connector 2) on a PX5. The top trace shows the timing of the SCA data lines; they change state coincident with the rising edge of the strobe.



The timing shown is with the clock set to 20MHz. The strobe high and low times are 200nS, as is the minimum idle time between events (i.e. the strobe low time after the 2nd strobe, and before the 1st strobe of the next event.) In reality, this idle time is governed by the peaking time – the minimum peaking time @ 20MHz is 800nS, and therefore the minimum idle time at 20MHz is approximately 800nS. The actual idle time is governed by the configured peaking time.

With the clock set to 80MHz, the signals are 4x faster – the strobe high and low times become 50nS. The minimum peaking time @ 80MHz is 50nS, so the minimum idle time between events is also 50nS.

The streaming mode uses SCA8 internally as the event source, so SCA8 must be enabled for streaming to operate. The SCA8 thresholds default to the entire spectrum, but they can be adjusted to focus on a ROI, remove the top or bottom of the spectrum, etc.

The events output in streaming mode are those that are accepted by SCA8. They are conditioned by the slow threshold, the SCA8 thresholds, PUR (if enabled), RTD (if enabled), detector reset (if enabled), and GATE (if enabled). The presets (acquisition time, real time, counts) do not affect SCAs (and therefore the streaming mode), nor does the LLD setting.

The streaming mode is enabled by sending the ASCII commands 'AUO2=STREAM;' and 'SCAI=8;'. [Setting the SCA index to 8 enables SCA8.] Additionally, on the PX5 or DP5G, the command 'CON2= AUXOUT2;' is needed to route the streaming strobe to connector 2.

6.3 Sequential buffer operation

The Sequential Buffer mode of operation causes a series of spectra and associated status data to be placed in an on-board memory for later retrieval. The buffering can be initiated either via a software command (see sections 4.1.3 and 4.1.4) or via a hardware signal (see sections 4.1.40 and 4.1.41). After buffering is complete, the buffers can be read out with a series of 'request buffer' commands (see section 4.1.5), which returns data in the same format as a normal 'Spectrum + status' response packet (see sections 4.2.2 - 4.2.13.)

For software application-controlled buffering, the 'Buffer Spectrum', 'Buffer & clear spectrum', and 'Request buffer' request packets are used. For hardware-controlled sequential buffering, the 'Restart sequential buffering', 'Cancel sequential buffering' and 'Request buffer' request packets are used.

[Note: Buffer Slot 0 is used by the standard Spectrum Request packets (see section 4.1.2). If a Spectrum Request packet is received before slot 0 has been read out, the contents of slot 0 will be overwritten by the current spectrum.]

Note that it is possible to use the GP Counter as a timebase or other indicator for the series of acquisitions. The source for the GP Counter could be set to AUX_IN1, and a high-frequency signal (for example) could be connected to the AUX_IN1 input. If the GP Counter is configured such that it is not disabled or cleared with the MCA ('GPMC=OFF;GPME=OFF;'), then the GP Counter will continue to increase even though the acquisition is cleared after each buffer is created. The value of the GP Counter in each slot's status packet will reflect the state of the GP Counter when that buffer was created, i.e. at the end of each sequential acquisition.

[Note that if the GP Counter is not cleared when the MCA is cleared, then a software command should be issued to clear the GP Counter when the run is started, or it will simply increment continuously.]

[Also note that if the GP Counter source is set to AUX_IN2, then the value of the GP Counter in the buffered status packet should contain the same value as the slot number in status offsets 46-47.]

The number of buffer slots available depends on the number of channels for which the device is configured:

Number of Channels	Number of buffer slots
256	512
512	256
1024	128
2048	64
4096	32
8192	16

Copying the spectrum and status to the buffer takes a finite amount of time, and that time depends on the FPGA clock rate and the number of channels selected. This table is copied from Section 3.4. During the time that the buffer is being copied, the acquisition is disabled.

	Time to buffer spectrum + status	
# of Channels	20MHz Clock	80MHz Clock
256	228uS	113uS
512	420uS	189uS
1024	804uS	343uS
2048	1.57mS	650uS
4096	3.12mS	1.27mS
8192	6.18mS	2.50mS

6.3.1 Software-controlled Sequential Buffer Operation

Software-commanded buffering can occur at any time – there is no specific mode for this. The 'Buffer Spectrum' and 'Buffer & clear spectrum' request packets cause the current spectrum to be copied into the buffer slot specified by the request packet. A buffer is read out via the 'Request Buffer' request packet. Note that buffer slot 0 is used by the normal 'Spectrum Request' packets, so one of these requests will overwrite whatever is stored in slot 0.

6.3.2 Hardware-controlled Sequential Buffer Operation

Hardware-controlled buffering is initiated by the 'Restart sequential buffering' request packet. It will continue until all buffer slots are full, or until the 'Cancel sequential buffering' request packet is received.

The status of the buffering operation can be monitored by periodically reading a Status packet – the values in offsets 46-47 indicate the next buffer slot to be used, and also include a flag that shows whether buffering is still active, or if it has been stopped because all buffers are full (or because a 'Stop sequential buffering' command was issued.) Note that this status value is part of the status packet that is recorded with each buffer operation – this value will show 'slot 0' in the data that is recorded in slot 0, 'slot 1' in the data recorded in slot 1, etc.

The hardware signal should be connected to the AUX_IN2 input. (For the PX5 and DP5G+PCG, the 'CON2=AUXIN2;' configuration command should be used to select the AUXIN2 input for the AUX-2 connector.) For the DP5, AUX_IN2 appears on the AUX connector, pin 11.

The buffer action is triggered by the rising edge of the signal. Its period should be greater than the buffer time listed above, and the minimum positive pulse width is 400nS.

The regular 'Request Spectrum' transfers are disabled while hardware sequential buffering is active. A 'Request Spectrum' request packet will return a BUSY ACK packet until the sequential buffering is complete or cancelled.

If the hardware signal is used with the PX5, the PX5 will chime when the buffers are full.