PX5 User Manual and Operating Instructions

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Other PX5 related documents:

- **PX5 Quick Start Guide**
- **DP5 Programmer's Guide**
- **WINUSB Installation Instructions**

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1 INTRODUCTION

The PX5 is a high performance digital pulse processor and power supply module. It is a component in a complete nuclear spectroscopy system, which must also include a detector and preamplifier. A complete system can be assembled by combining the PX5 with one of Amptek's detectors and preamps (several options and configurations may be used) or a user can supply his own detector and preamplifier, and/or power supply. The PX5 is similar in many ways to a combination of Amptek's DP5 signal processor and PC5 power supply module, but has several enhancements and is packaged for laboratory use. The DP5 and PC5 are printed circuit board assemblies, suited primarily to OEM applications as part of a complete system.

The PX5 is designed primarily for use with high resolution solid state detectors. It works very well with Amptek's SDD, SiPIN, and CdTe X-ray detectors. A variant (with custom power supplies) yields high performance with HPGe γ-ray detectors.

The PX5 is a digital pulse processor (DPP) which replaces both the shaping amplifier and MCA found in analog systems. The digital technology improves several key parameters: (1) better performance, specifically better resolution and higher count rates; (2) greater flexibility since more configuration options are available, selected by software, and (3) improved stability and reproducibility. The DPP digitizes the preamplifier output, applies real-time digital processing to the signal, detects the peak amplitude, and bins this in its histogram memory. The spectrum is then transmitted to the user's computer.

The PX5 includes all power supplies necessary to operate Amptek's detectors. Operating off +5 VDC, it produces high voltage (commandable over a +/-1500V range), low voltages for the preamps, and provides close loop control for the thermoelectric cooler.

The PX5 supports USB, RS232, and Ethernet, and the auxiliary connectors provides several additional inputs and outputs. This includes a DAC output, an MCA gate, timing outputs, eight SCA outputs, and others. The PX5 is supplied with the DPPMCA data acquisition and control software, along with interface subroutines to integrate the unit with custom software (DPP FW6 SDK). Optional accessories include software for analyzing X-ray spectra, several collimation and mounting options, vacuum accessories, and X-ray tubes to complete a compact system for X-ray fluorescence (XRF).

Figure 1-1. Photograph of PX5 front (top) and back (bottom).

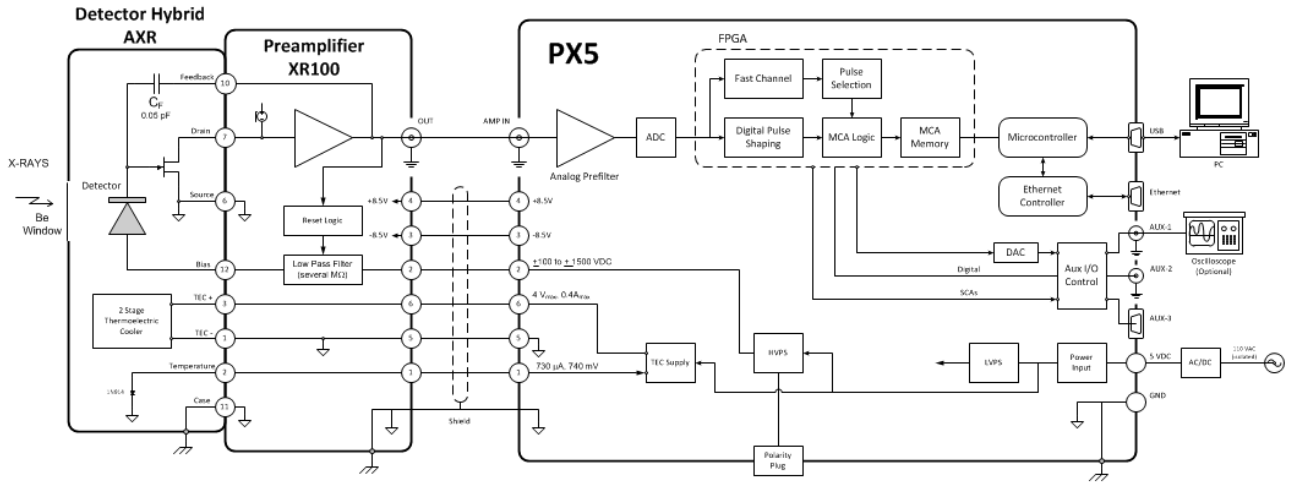


Figure 1-2. Block diagram of the PX5 connected to an Amptek XR100 detector.

Understanding Signal Processing in the PX5

A complete, typical nuclear spectroscopy system includes a few key components: (1) the detector, (2) the preamplifier, (3) the pulse processing electronics (which include pulse shaping, pulse selection logic, pulse counters, a multichannel analyzer, and interfaces for data acquisition and control), (4) the power supplies, (5) the packaging or enclosure for the system, and (6) the computer running software for instrument control, data acquisition, and data analysis. The PX5 is a single board digital pulse processor which implements the functions described in (3). As a packaged solution, it is most appropriate for laboratory users (OEM integration frequently utilize a DP5 and PC5). This section of the User's Manual provides some background information on the signal processing in the PX5. Later sections will provide detailed specification and application information.[1]

[1] This section presumes familiarly with radiation detection. For additional information, we recommend:

G.F. Knoll, *Radiation detection and measurement*, 3rd edition, John Wiley & Sons, 2000.

H. Spieler, *Semiconductor detector systems*, Oxford University Press, 2005.

R. Jenkins, R.W. Gould, D. Gedcke, *Quantitative X-ray spectrometry*, 2nd edition, Marcel Dekker, Inc., 1995.

G. Gilmore, J. Hemingway, *Practical gamma-ray spectrometery*, John Wiley & Sons, 1995.

2 MAJOR FUNCTION BLOCKS

Figure 2-1 shows how a Digital Pulse Processor (DPP) is used in the complete signal processing chain of a nuclear instrumentation system and its main function blocks. The DPP digitizes the preamplifier output, applies real-time digital processing to the signal, detects the peak amplitude (digitally), and bins this value in its histogramming memory, generating an energy spectrum. Pulse selection logic can reject pulses from the spectrum using a variety of criteria. The spectrum is then transmitted over the DPP's USN, RS232, or Ethernet interface to the user's computer.

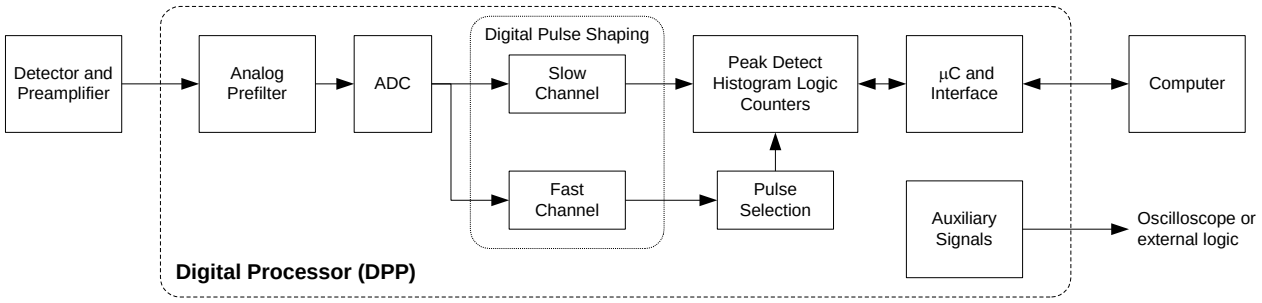


Figure 2-1. Block diagram of a Digital Pulse Processor (DPP) in a complete system.

Analog Prefilter: The input to a standard PX5 is the output of a charge sensitive preamplifier. The analog prefilter circuit prepares this signal for accurate digitization. The main functions of this circuit are (1) applying appropriate gain and offset to utilize the dynamic range of the ADC, and (2) carrying out some filtering and pulse shaping functions to optimize the digitization.

ADC: The 12-bit ADC digitizes the output of the analog prefilter at a 20 or 80 MHz rate. This stream of digitized values is sent, in real time, into the digital pulse shaper.

Digital Pulse Shaper: The ADC output is processed continuously using a pipeline architecture to generate a real time shaped pulse. This carries out pulse shaping as in any other shaping amplifier. The shaped pulse is a purely digital entity. Its output can be routed to a DAC, for diagnostic purposes, but this is not necessary.

There are two are two parallel signal processing paths inside the DPP, the "fast" and "slow" channels, optimized to obtain different data about the incoming pulse train. The "slow" channel, which has a long shaping time constant, is optimized to obtain accurate pulse heights. The peak value for each pulse in the slow channel, a single digital quantity, is the primary output of the pulse shaper. The "fast" channel is optimized to obtain timing information: detecting pulses which overlap in the slow channel, measuring the incoming count rate, measuring pulse risetimes, etc. and to obtain

Pulse Selection Logic: The pulse selection logic rejects pulses for which an accurate measurement cannot be made. It includes pile-up rejection, risetime discrimination, logic for an external gating signal, etc.

Histogram Memory: The histogram memory operates as in a traditional MCA. When a pulse occurs with a particular peak value, a counter in a corresponding memory location is incremented. The result is a histogram, an array containing, in each cell, the number of events with the corresponding peak value. This is the energy spectrum and is the primary output of the DPP. The unit also includes several counters, counting the total number of selected pulses but also counting input pulses, rejected events, etc. Auxiliary outputs include eight different single channel analyzers, and both a DAC output and two digital outputs showing pulse shapes selected from several points in the signal processing chain.

Interface: The PX5 includes hardware and software to interface between these various functions and the user's computer. A primary function of the interface is to transmit the spectrum to the user. The interface also controls data acquisition, by starting and stopping the processing and by clearing the histogram memory. It also controls certain aspects of the analog and digital shaping, for example setting the analog gain or the pulse shaping time. The DPP includes USB, RS232, and Ethernet interfaces.

Power: The PX5 also includes a power interface. It takes a loosely regulated +5 VDC input and generates the various levels required by the signal processing circuitry (+/- 5.5 V, 3.3 V, 2.5 V). It also generates the

levels required by the detector and preamplifier (bias voltage of +/- 1500 V, preamp power up to +/-8.5 V, and power for the thermoelectric cooler providing closed loop temperature control).

2.1 ANALOG PREFILTER

The PX5 was designed to process signals coming directly from a charge sensitive preamplifier used with solid-state radiation detectors. These signals typically have (1) a small amplitude, in the range of a few mV, (2) a fast rise (tens of nsec to μsec), and (3) the small pulses "ride up" on one another as the signal pulses accumulate. These steps can be seen in the top traces of Figure 2-2 and are not suitable to be directly digitized, due to the small amplitude (a few mV) over the large range (many volts). The analog prefilter prepares the signal so it can be accurately digitized.

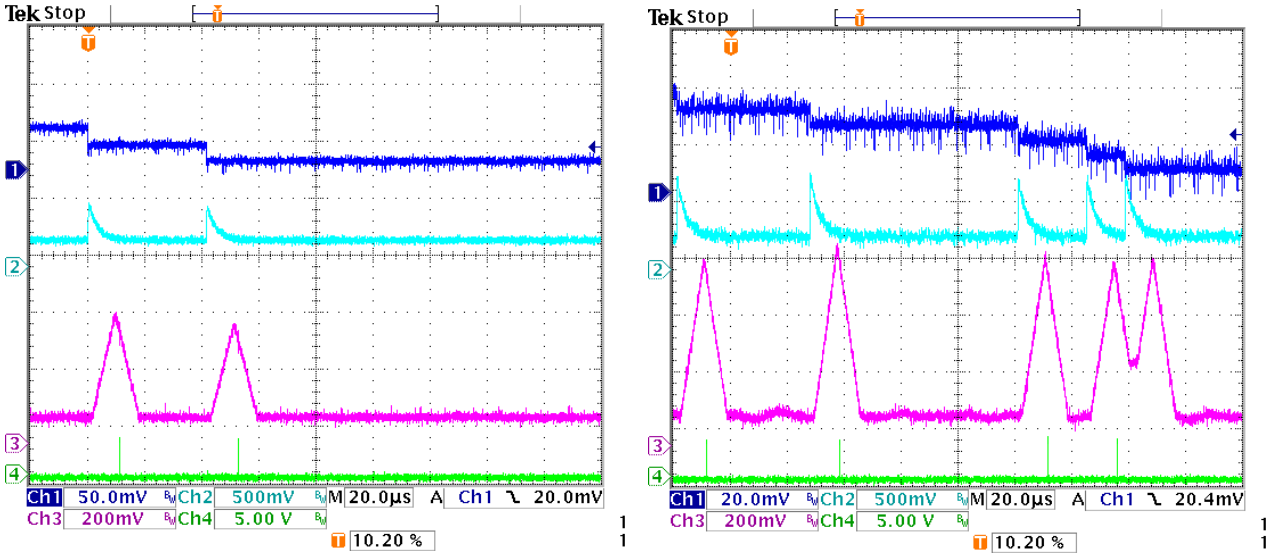


Figure 2-2. Oscilloscope traces illustrating the signal processing. The dark blue trace on top shows the output of the preamplifier: a series of "steps" of a few millivolts, spaced randomly in time. High frequency white noise is clearly superimposed. The traces on the left (right) were measured with 60 (5.9) keV X-rays. The signal to noise ratio is clearly much degraded on the right. The light blue traces show the output of the analog prefilter, with its 3.2 μsec pole. The magenta trace shows the shaped output: it is the peak of this which is detected and is binned in the spectrum. The green trace is a logic output indicating that a valid peak has been detected.

The prefilter implements three functions: (1) it applies a high pass filter with a 3.2 μsec time constant, so that the pulses no longer "ride up" on one another, (2) it applies a coarse gain so that the largest pulses are approximately 1 V (to maximize the ADC resolution), and (3) it applies a DC offset so that the signal always falls within the range of the unipolar ADC. The output of the prefilter can be seen as the cyan color trace in Figure 2-2 and consists of a series of pulses with a fast rise, 3.2 μsec decay, a baseline of a few hundred millivolts, and maximum values of around 1V. The prefilter can accommodate pulses of either polarity, inverting the signals digitally. For opposite polarity signals, the prefilter output will have a baseline of approximately 1.8 V, with negative steps of magnitude approximately 1 V.

Amptek's detectors generally utilize a pulsed reset but the PX5 analog prefilter includes a pole zero cancellation circuit for preamps with continuous feedback. It can accommodate time constants down to 50 μs. The PX5 also includes a second high pass filter, with a 1.6 μs time constant. This improves performance at high rates but degrades performance at long peaking times. It is recommended at input count rates above 200 kcps.

System Gain

The system conversion gain is expressed in units of channels/keV: it gives the MCA channel number in which a particular energy peak will occur. It is the product of three terms: (1) the conversion gain of the charge sensitive preamplifier (in units of mV/keV), (2) the total gain of the voltage amplifier (the product of coarse gain and fine gain), and (3) the conversion gain of the MCA (channels per mV).

For Amptek's XR100CR detectors, the preamp conversion gain is typically about 1 mV/keV. The MCA's conversion gain is given by the number of channels selected (for example, 1024) divided by the voltage corresponding to the peak channel. In Amptek's digital processors, this is approximately 950 mV. The DPP gain is the product of the coarse and fine gains. For example, if the fine gain is 1.00 and the coarse gain is 66.3, then the system conversion gain is (1 mV/keV)(66.3)(1.00)(1025 ch/950 mV)=71.5 channels/keV. The inverse of this is the MCA calibration factor, 14 eV/channel. The full scale energy is 1024 channels/71.5 channels per keV, or 14.3 keV. Note that these values are approximate. Due to manufacturing tolerances in the feedback capacitors, in resistors, etc the actual gain can vary by several percent, which will cause a noticeable shift in the spectrum. These calculations should be used for system design and for initial configuration. For any given system, the user must tune the gain and calibrate the spectrum. For systems other than Amptek's XR100 series, the preamp conversion gain can be estimated. It is the product of three terms: (1) one over the energy required to create an electron hole pair in the detector (W), (2) any internal detector gain, e.g. with a proportional counter or PMT, and (3) the preamp's conversion gain, q/C_F, where C_F is the feedback capacitance. For example, for a Xe proportional counter, W is 21.5 eV. At a gain of 10^3 and C_F=1 pF, the conversion gain is (1/21.5 eV/pair)(10^3)(1.6x10^{-19} C/10^{-12} F)=7.4 mV/keV.

Reset and Continuous Preamplifiers

Most spectroscopy detectors utilize a charge sensitive preamplifier which precedes the analog prefilter in the PX5. A charge sensitive preamplifier produces a voltage proportional to the time integral of the current. The integrator will eventually saturate because the time integral of the current through the diode continues to increase. There are two methods used to keep the preamplifier output within range: resets and continuous feedback. Figure 2-3 (left) shows the output of a reset preamp over a very long time: many small steps of a few mV each causes the output to linearly approach the negative limit (-5 V) in a time of several seconds. The reset pulse occurs so the output goes to the initial value (+5 V) in a few μsec. Reset preamplifiers provide the minimum electronic noise and so are used in Amptek's lowest noise systems, including the XR100. The very large transient created during reset can affect signal processing, so the DPP includes logic to "lock out" the effects of this reset.

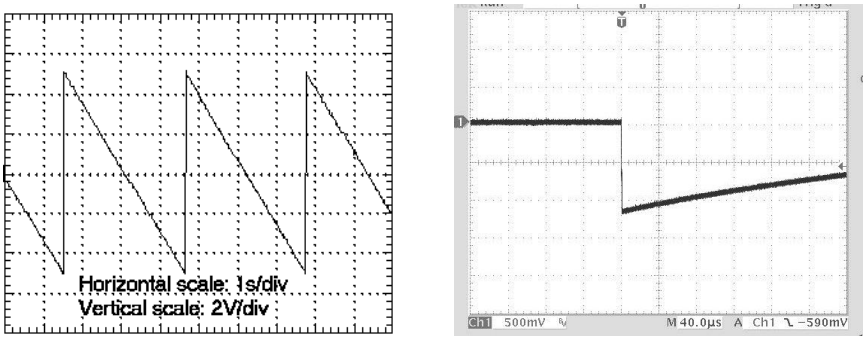


Figure 2-3. Oscilloscope traces showing typical preamplifier outputs, for reset preamps (left) and for continuous feedback preamps (right).

Another traditional solution is to add a slow feedback path which restores the input to a value near ground In the simplest case, a feedback resistor R_F is placed in parallel with the feedback capacitor C_F on which the current is integrated. After the voltage step ΔV due to each signal interaction, the output slowly drifts back to its quiescent value, with the time constant of the feedback, as illustrated in Figure 2-3 (b). This time constant is 500 μsec in this plot. The long time permits accurate integration of the total charge but causes the pulses to pile-up on one another. The feedback resistor adds electronic noise so is not used in the lowest noise systems. Some Amptek detectors replace the feedback resistor with a transistor. This offers lower noise than resistive feedback but does not match the performance of the reset preamps.

2.2 PULSE SHAPING

Slow Channel

The "slow channel" of the DPP is optimized for accurate pulse height measurements. It utilizes trapezoidal or cusp pulse shaping, with a typical output pulse shape shown in Figure 2-4. This shape provides a near optimum signal to noise ratio for many detectors. Relative to conventional analog shapers, the trapezoid provides lower electronic noise and, simultaneously, reduced pulse pile-up.

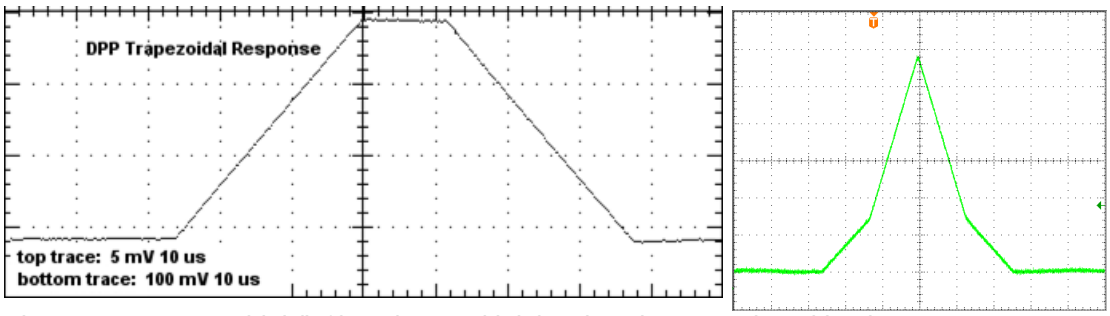


Figure 2-4. Trapezoidal (left) and Cusp (right) pulse shape produced by the DPP.

The user can adjust the rise/fall time (the rise and fall must be equal) and the duration of the flat top over many steps. A semi-Gaussian amplifier with shaping time τ has a peaking time of 2.4τ and is comparable in performance with the trapezoidal shape of the same peaking time. A DPP with 2.4 μsec peaking time will be roughly equivalent to a semi-Gaussian shaper with a 1 μsec time constant.

Adjusting the peaking time is a very important element in optimizing the system configuration. There is usually a trade-off: the shortest peaking times minimize dead time, yielding high throughput and accommodating high count rates, but the electronic noise usually increases at short peaking times. The optimum setting will depend strongly on the detector and preamplifier but also on the measurement goals. The electronic noise of a detector will generally have a minimum at some peaking time, the "noise corner." At peaking times shorter or longer than this, there is more noise and hence degraded resolution. If this peaking time is long relative to the rate of incoming counts, then pulse pile-up will occur. In general, a detector should be operated at a peaking time at the noise corner, or below the noise corner as necessary to accommodate higher count rates.

If the risetime from the preamp is long compared with this peaking time, then the output pulses will be distorted by ballistic deficit. In this case, the trapezoidal flat top can be extended to improve the spectrum. The specific optimum timing characteristics will vary from one type of detector to the next and on the details of a particular application, e.g. the incoming count rate. The user is encouraged to test the variation of performance on these characteristics.

Fast Channel

The DPP's "fast channel" is optimized to detect pulses which overlap in the "slow channel". The fast channel is used for pile-up reject logic (rejecting pulses which are so closely spaced that they cannot be distinguished in the slow channel) and for determining the true incoming count rate (correcting for events lost in the dead time of the slow channel). The fast channel also utilizes trapezoidal shaping, but the peaking time is commendable to either 100 nsec or 400 nsec. The oscilloscope traces in Figure 2-5 show the measured pulse shapes with a 100 nsec peaking time. As seen on the right, pulses which are separated by only 120 nsec are separately counted in the fast channel.

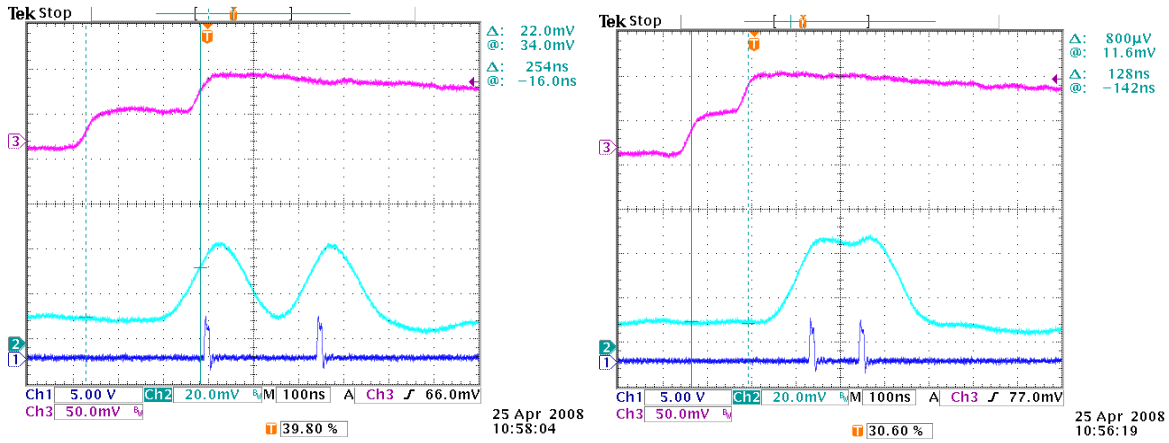


Figure 2-5. Oscilloscope traces showing operation of the DPP "fast channel". The magenta trace at top shows the ADC input, the light blue trace shows the fast channel shaped output, and the dark blue trace shows the logic output which counts the fast channel events.

Baseline Restoration

The pulse height is implicitly measured relative to a baseline. Any random fluctuation or systematic variation in the baseline, whether high frequency noise or a slow change, will degrade the pulse height measurement. The baseline is often assumed to be "ground", but this is a somewhat ambiguous notion, since "ground" represents simply the reference for voltage measurements. If this baseline changes with time, count rate, or anything else, then distortions are introduced into measurements. In pulse height analysis, the spectrum will appear to shift, while in counting systems, the threshold will change. In practice, the most common baseline shift occurs with count rate.

The peak of the "baseline" of a digital processor has some significant differences from traditional analog shaping amplifiers. Because the DPP's transfer function has a finite impulse response, after a pulse has passed through the processing pipeline it has no impact on the output. This is fundamentally different from an analog differentiator and results in vastly enhanced baseline stability at high count rates. However, unlike analog shapers the DPP has to establish a DC baseline, at all count rates, and in practice some shifts with count rate are observed.

The DPP has an asymmetric baseline restorer with several different settings. The DPP BLR uses the negative peaks from random noise to determine the baseline. The negative-going noise peaks only occur in the absence of a signal, so if these are stable, then the baseline is stable, independent of counts. The BLR generally produces an offset comparable to the rms noise value. There are two independent parameters, UP and DOWN, each of which can be set to four values: Very Slow, Slow, Medium, and Fast. These are essentially slew rates in the baseline response. A setting of Very Fast for both UP and DOWN means that the BLR will respond very rapidly to any measured variation in the baseline. It must be stressed that the optimum setting depends strongly on the details of a particular application: the nature of the baseline drifts, etc. If the peaks are found to shift to lower channels at high count rates, then increase the UP slew rate or decrease the DOWN slew rate. If one observes occasional "bursts" in the system which cause the spectrum to shift to higher channels (often manifesting as bursts of noise above the threshold), then decrease the UP slow rate or increase the DOWN slew rate.

2.2.2 Pulse Selection

Thresholds

The DPP uses thresholds to identify pulses. Both fast and slow channels have their own independent thresholds. Noise is usually higher in the fast channel, and it is best to set the thresholds just above the noise, so they will be different in the two channels. The DPP uses the Slow Channel Threshold to identify events that should be added to the stored spectrum. Events with an amplitude lower than the Slow Channel Threshold are ignored – they do not contribute to the stored spectrum. The slow channel threshold is the equivalent of a low-level discriminator (LLD).

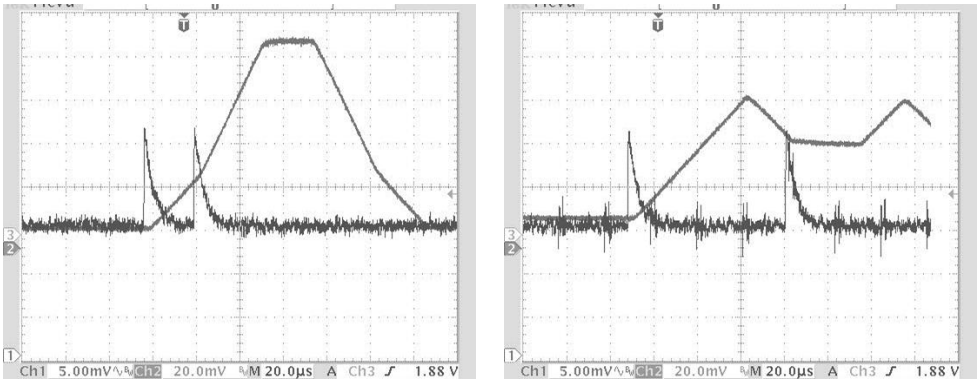
The Fast Channel Threshold also functions as an LLD and is used for several functions. (1) The rate of events over the fast threshold is the DPP's measurement of the incoming count rate (ICR). (2) Pile-Up Rejection (PUR) logic identifies events which overlap in the slow channel but are separated in the fast channel. (3) Rise Time Discrimination (RTD) uses the amplitude of the fast channel signal to measure the current at the beginning of a pulse. PUR and RTD are discussed in more detail below.

Properly setting these thresholds is very important for getting the best performance from the DPP. Under most circumstances, the thresholds should be set just above the noise, and the DPPMCA software includes an "AutoTune" function to set these. Improperly set thresholds are responsible for a large number of problems reported by customers. If the fast channel threshold is too low, for example, and PUR is enabled, then every event will be rejected and so there appears to be no signal. If the slow channel threshold is too high, then it is also possible to reject all events.

Pile-Up Rejection

The goal of the pile-up reject (PUR) logic is to determine if two interactions occurred so close together in time that they appear as a single output pulse with a distorted amplitude. The DPP PUR uses a "fast-slow" system, in which the pulses are processed by a fast shaping channel in parallel with the slower main channel (both channels are purely digital). Though similar in principle to the techniques of an analog shaper, the pile-up reject circuitry and the dead time of the DPP differ in significant ways, resulting in much better performance at high count rates. First, the symmetry of the shaped pulse permits the dead time and pile-up interval to be much shorter. Second, there is no dead time associated with peak acquisition and digitization, only that due to the pulse shaping.

Figure 2-6 illustrates the operation of the DPP for pulses that occur close in time. Figure 2-6 (a) shows two events that are separated by less than the rise time of the shaped signal, while Figure 2-6 (b) shows two pulses that are separated by slightly longer than the rise time. In (a), the output is the sum of the two signals (note that the signal amplitude is larger than the individual events in (b)) and the events are said to be piled up. However, note that the analog prefilter outputs in (a) are separate. For a nearly triangular shape, pile-up only occurs if the two events are separated by less than the peaking time, in which case a single peak is observed for the two events. The interval used by the DPP for both dead time and pile-up rejection is the sum of risetime and the flat-top duration. If two events occur within this interval and pile-up rejection is disabled, then the single, piled-up value is in the spectrum. If pile-up rejection is enabled and two events are separated by more than the fast channel pulse pair resolution (120 nsec) and less than this interval, both are rejected. Events that exceed a threshold in the fast channel trigger the pile-up reject logic.



(a) (b)

Figure 2-6. Oscilloscope traces illustrating the dead time and pile-up reject performance of the DPP

Reset Lockout

As discussed previously, many preamps use pulsed reset to prevent saturation of the preamp output. The reset generates a very large signal in the DPP, causing its amplifiers to saturate, registers to overflow, etc. The DPP therefore includes a reset detect circuit (which detects a very large, negative going pulse) and logic to lock out signal processing for some time following the reset, to give time for everything to return to stable values. The DPP permits the user to enable or disable reset (it should be disabled for preamps with continuous feedback). The user can also select the time interval during which the signal is locked out. If the interval chosen is too short, then there will be some distortion of the waveform (and thus spectrum) following

reset. At high count rates the reset pulses occur frequently, and if the interval chosen is too long, then a significant dead time is observed.

Risetime Discrimination

In some types of applications it is important to separate pulses based on the duration of the transient current through the detector, into the preamplifier. For example, in some Si diodes there is an undepleted region with a weak electric field. A radiation interaction in this region will generate a signal current, but the charge motion is slow through the undepleted region. These interactions in this region can lead to various spectral distortions: background counts, shadow peaks, asymmetric peaks, etc. In CdTe diodes, the lifetime of the carriers is so short that slow pulses exhibit a charge deficit, due to trapping. These lower amplitude pulses distort the spectrum. In scintillators, pulse shape discrimination is sometime used to differentiate gamma-rays and neutrons. This pulse shape discrimination can be implemented using the DPP's RTD function. Most Amptek detectors do not require or benefit from RTD but for some it is quite useful.

Risetime discrimination rejects from the spectrum events with a long detector current, which leads to a slowly rising edge in the fast and slow shaped pulses. Amptek's DPP implements RTD by comparing the peak height in the fast channel (which samples the charge integrated in the first 100 nsec) to the peak height in the slow channel (which samples the charge which is eventually integrated). If this ratio is sufficiently high, the risetime was fast and thus the pulse is accepted. If this ratio is low, the pulse is rejected. Because the fast channel is inherently much noisier than the slower shaped channel, an RTD threshold is also implemented on the shaped channel. Events which fall below this threshold (the "RTD Slow Threshold") are not processed by the RTD and are thus accepted (unless otherwise rejected by Pileup Rejection or some other criterion). Because RTD is most often needed on interactions deep in a detector, arising from high-energy events, low-amplitude events are unlikely to benefit from RTD rejection. These fall below the RTD Slow Threshold and are thus accepted.

Gate

The gate input is used with external circuitry to determine if events should be included or excluded from the spectrum. The gate can be active high or active low (or disabled). If disabled, then this input is ignored and all events (which meet the criteria above) are counted. If active high (low), then if the gate input is high (low), the event is counted in the spectrum. When counts are gated off, the clock accumulation time counter is also gated off so that an accurate count rate can be determined. The timing of this gate input is important. If the gate input is active while the fast channel threshold is triggered, then the event is counted as a fast count. If the gate input is active when the peak detect is triggered, then the event is counted as a slow count and shows up in the spectrum. Note that the fast and slow channels are triggered at different times, since they have different shaping times.

2.2.3 MCA, MCS, Counters, and SCAs

Multichannel Analyzer

The Multichannel Analyzer (MCA) operates like a conventional MCA except that the input is already digitized. It detects the amplitude of the peak of the shaped pulse using a digital peak detect circuit. If the selection logic indicates that the pulse is valid, then it increments the value stored at a memory location corresponding to the peak amplitude. The MCA supports 256, 512, 1024, 2048, 4096 or 8192 channels. The DPP uses 3 bytes per channel, which allows up to 16.7M counts per channel.

The MCA hardware in the PX5 can be started and stopped by commands over the serial bus. It can also be preset to stop after a programmed acquisition time (with a minimum of 100 milliseconds) or after a programmed number of counts has been measured within the SCA8 region of interest (see below).

Acquisition Time

The DPP measures the spectrum and counts during the "acquisition time", which is also measured and reported. The acquisition time is the real elapsed time during which data are being acquired. The acquisition time clock is turned off during certain events, including data transfers over the serial bus and including reset intervals. If a reset preamplifier is used, and the DPP is configured for a certain reset time period, then acquisition is shut down during the reset period and the acquisition clock is stopped. This acquisition time is measured using a typical 50 ppm crystal oscillator so is quite accurate. The true count rate should be computed using the actual acquisition time rather than the nominal data transfer time.

Data transfers occur based on an approximate real time clock in the host PC. For example, one might configure DPPMCA to acquire data from the DPP every second. When the data transfer occurs, the acquisition time is shown and this will probably differ from the nominal "1 second", due to the approximate clock and also due to reset losses. (A typical value is 1.05 second.) At high count rates, a reset preamp resets more often, and so there is less acquisition time per transfer. In this case, the acquisition time might become 0.85 seconds. On the screen, this time is displayed along with the fast counts and the slow counts during the same interval. The actual count rate is found by dividing the observed counts by the observed acquisition time, 0.85 seconds for this example.

Dead Time

All nuclear spectroscopy systems exhibit a dead time associated with each radiation interaction. Following any interaction, there will be a time period during which subsequent pulses cannot be detected and will not contribute to the output counts. Because the timing of pulses is random, there is always some probability that pulses will occur in these dead time intervals, and therefore the output count rate (R_{out}) measured by a system is always lower than the input count rate (R_{in}). The measurement goal is to determine the incident spectrum and count rate, which requires correcting for these losses.

The dead time characteristics of a digital processor differ considerably from those of more traditional analog systems. This is discussed in some detail in an Amptek application note and a research publication. Some key points are:

- The deadtime per pulse of a digital processor is lower than that of a comparable analog system. There is no deadtime associated with acquiring the peak (this is termed simply the deadtime in an analog MCA and often dominates system deadtime) and the deadtime per pulse is greatly reduced due to the finite impulse response of the shaping.
- The best way to determine the incoming count rate is to directly measure it, using the DPP's fast channel. The accuracy and precision of this method are much better than that obtained using livetime clocks, which are traditional for analog systems, under most circumstances.
- The DPPMCA software estimates the DPP deadtime by comparing the count rates in the fast and slow channels. We recommend keeping this value below 60%. The DPP operates at higher deadtime losses and can yield very accurate results, but great care is required in configuring the system and interpreting the count results.

Counters

The DPP has several counters which are started and stopped at the same time as the spectrum. This includes the "fast channel counter", which records all fast channel events which exceed the fast channel threshold. Note that there is no upper limit, and that none of the pulse selection logic applies (this is gated off during reset and data transfer). The slow channel counter records all events which are recorded in the spectrum. Note that there is an upper limit: events exceeding the maximum pulse height channel are not in the spectrum, hence not in the slow counts. The full pulse selection logic applies (PUR, RTD, etc).

An additional counter records those events rejected by PUR and RTD. This is generally not of direct use but can be a "quality assurance" value by which one can verify system operation. The DPP also includes an external counter, an external TTL input to a counter which is started and stopped at the same time as the other counters. This is useful if, for example, one has a second detector and the counts at the same time are of interest.

Single Channel Analyzers

The PX5 contains eight single channel analyzers (SCAs). Each SCA has an upper and a lower threshold. If an event occurs with a shaped output within the range defined by these thresholds, and is accepted by PUR and the other pulse selection logic, then a logic pulse is generated and is output to the AUX connector, where it can be connected to external hardware. These are commonly used when a user needs to record count rates at a much higher time resolution than the 100 millisecond minimum for spectrum acquisition and only needs the rates within a few energy bands. The upper and lower limits of the 8 SCAs can be set independently in the software.

SCA8 serves a dual purpose – not only does it operate like the other SCAs, but it is also used to set the Region-of-Interest (ROI) for the Preset Count mode of MCA operation. That is, when a Preset Count is selected, the MCA will stop after the programmed number of counts occurs in the SCA8 ROI.

Multichannel Scaler

The Multichannel Scaler (MCS) produces spectral packets identical to those of the MCA, but they represent very different data. The MCS is used to measure total counts versus time rather than amplitude. Each "channel" in the spectrum represents a time interval. The MCS time base is commanded to a certain value, e.g. 0.5 sec. The system records all the counts in SCA8 during the first 0.5 second, writes this total into channel 1, records the counts in SCA8 during the second 0.5 second, writes this total into channel 2, and so on. The histogram memory can be used in either MCS or MCA mode (it cannot record in both modes simultaneously).

2.2.4 Electrical & Software Interfaces

There are three main elements to the electrical interface: communications, power, and auxiliary. The communications interfaces are the primary means to control the PX5 and to acquire the data. The PX5 supports USB, RS232, and Ethernet interfaces. With all three interfaces commands are issued to set the many configuration parameters. The unit sends three classes of data packets back to the computer: status packets (which include the counter outputs), spectral data packets (which contain the MCA output array), and oscilloscope packets.

Amptek's DPPMCA software provides the quickest way to control and readout the PX5. It provides access to all of the configuration parameters in the DPP, lets one start and stop data acquisition, reads and displays the data, performs very simple analyses, and saves the data in an ASCII format. The files saved by DPPMCA can be read by many spectral processing software packages.

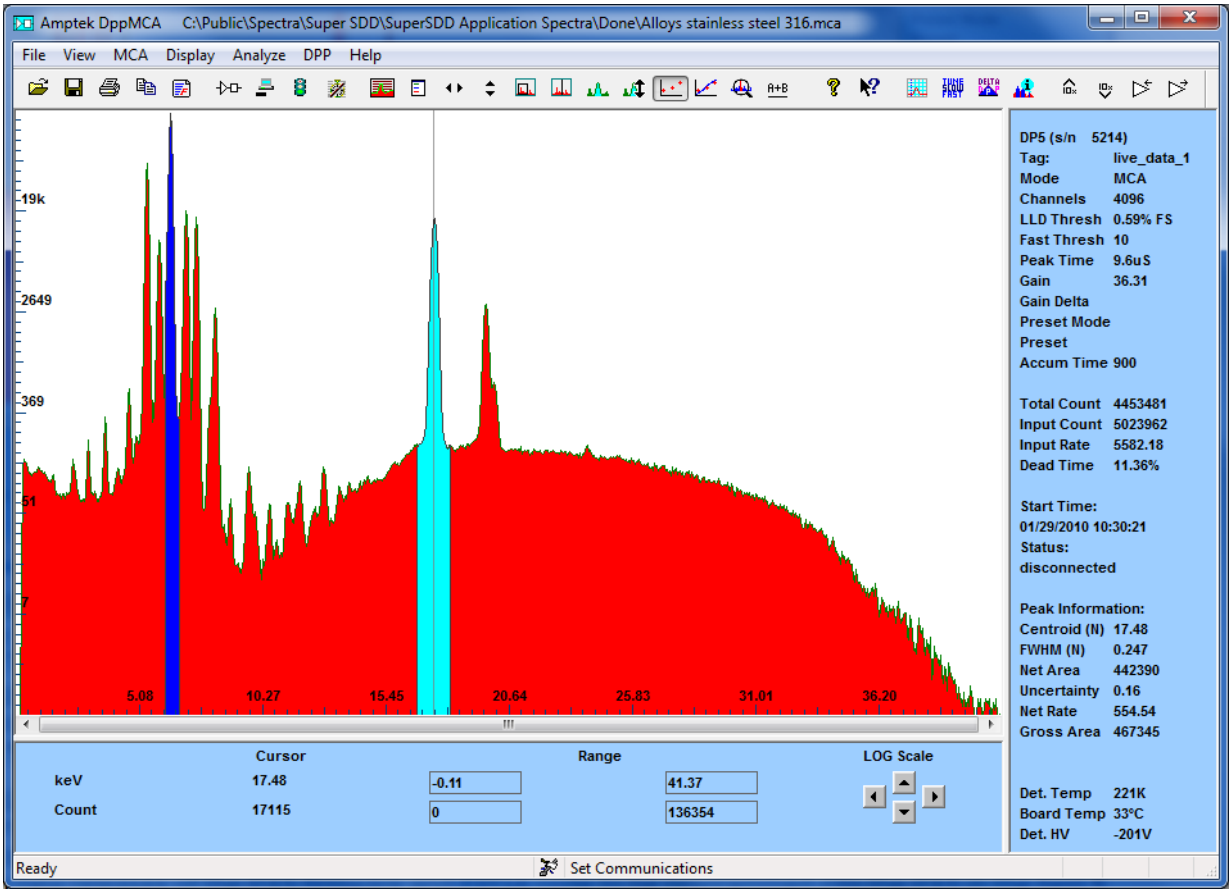


Figure 2-7. Typical screen display for DPPMCA. This shows the characteristic X-rays emitted by a stainless steel alloy, excited by a 40 kVp X-ray tube and measured by an SDD. The main window shows the spectral

display. The user has defined two regions of interest (ROIs). The panel on the right displays counts, acquisition time, key parameters, and data regarding the selected ROI (light blue. The toolbar along top contains a button to access the configuration parameters, along with other frequently used functions.

Amptek also provides a software developer's kit (DDP SDK) demonstrating subroutines which can be used to interface to the DPP. A user can incorporate these into custom software. A demonstration program written in Visual Basic and C++ is provided. Amptek also provides an "Upload Manager" permitting new releases of the firmware and FPGA code to be programmed into the PX5 in the field.

The auxiliary interface provides logic inputs and outputs which are not needed for the normal operation of the unit but which can be used for setup and debugging or for interfacing with external hardware. The PX5 includes two auxiliary outputs which can be commanded to show any of several signals. These are often displayed on an oscilloscope (along with the output of a DAC showing the signal processing in the FPGA) for setup and debugging. The SCA outputs are generally counted directly.

3 SPECIFICATIONS

Spectroscopic Performance: The spectroscopic performance (energy resolution, electronic noise, energy range, peak to background ratio, etc.) depends very strongly on the detector and preamplifier utilized.

Pulse Processor	
Gain Settings	Combination of coarse and fine gain yields overall gain continuously adjustable from 0.75 to 516.
Coarse Gain	28 log spaced coarse gain settings from x1 to x413
Fine Gain	Software selectable, 0.75 to 1.25, 10 bit resolution
Full Scale	1000 mV input pulse @ X1 gain
Gain Stability	<30 ppm/° C (typical)
ADC Clock Rate	20 or 80 MHz, 12 bit ADC
Pulse Shape	Trapezoidal or Cusp. (A semi-Gaussian amplifier with shaping time τ has a peaking time of 2.4τ and comparable performance with a trapezoidal shape of the same peaking time.)
Peaking Time	Software selectable peaking times between 0.05 and 102 µs, corresponding to semi-Gaussian shaping times of 0.02 to 43 µs.
Flat Top	Software selectable values for each peaking time (depends on the peaking time), > 0.05 nsec.
Maximum Count Rate	With a peaking time of 0.2 µs, 4 MHz periodic signal can be acquired.
Dead Time Per Pulse	1.05 times the peaking time. No conversion time.
Fast Channel Peaking Time	50, 100, 400 ns (80 MHz)
Fast Channel Pulse Pair Resolving Time	1.2 x Fast Channel Peaking Time (minimum of 60 nsec)
Pile-Up Rejection	Pulses separated by more than the fast channel resolving time and less than 1.05 x peaking time are rejected.
Baseline Restoration	Asymmetric, 16 software selectable slew rate settings
Dead Time Correction Displayed in Software	Manual correction based on Fast Channel measurement of ICR. Accurate to 1% for ICR < 1 Mcps under typical conditions.
Rise Time Discriminator (RTD)	The digital pulse processor can be programmed to select input pulses based on their rise time properties.
Gate	The gate input is used with external circuitry to determine if events should be included or excluded from the spectrum. The gate can be active high or active low (or disabled).

Multichannel Analyzer	
Number of channels	256, 512, 1024, 2048, 4096, or 8192 channels.
Bytes per channel	3 bytes (24 bits) - 16.7M counts
Acquisition Time	10 msec to 466 days
Data Transfer Time	1k channels in 4.8 milliseconds (USB) or 35 milliseconds (Ethernet)
Conversion Time	None.
Presets	Time, total counts, counts in an ROI, counts in a channel

MCS Timebase	10 millisec/channel to 300 sec/channel
External MCA Controls	Gate input: Pulses accepted only when gated on by external logic. Input can be active high or active low. Software controlled.
Counters	Slow channel events accepted by MCA, Incoming counts (fast channel counts above threshold), SCA8 counts, event rejected by selection logic, and external event counter. Sixteen ROI counters.

Hardware	
Microprocessor	Silicon Labs 8051F340 (8051-compatible core)
External Memory	512kB low-power SRAM
Firmware	Signal processing is programmed via firmware, which can be upgraded in the field.

Communications
USB 2.0 full speed (12 Mbps)
RS-232 at 115.2k or 57.6k baud
Ethernet standard 10base-T

Connections	
Analog Input (BNC)	The analog input accepts positive or negative going pulses from a charge sensitive preamplifier.
Power	+5 VDC. Mates with a center positive 5.5 mm x 2.1 mm power plug.
USB	Standard USB mini-b jack.
Ethernet	Standard Ethernet jack.
AUX-1 (BNC)	Configured in software as (1) an analog output, to view shaped pulses or diagnostic signals, (2) a digital output, to view a discriminator output or diagnostic signals, or (3) a digital input.
AUX-2 (BNC)	Configured in software as (1) a digital output, to view a discriminator output or diagnostic signals, or (2) a digital input, to gate or synchronize data acquisition.
AUX-3 (15 pin D connector female)	Includes (a) the lines for a serial RS232 interface, (b) two lines which can be configured for digital inputs or outputs, (c) 8 single channel analyzer (SCA) outputs, and (d) a control line to command the power on or off remotely.

Power	
+5 V	+5 VDC at 500 mA (2.5 W) typical. Current depends strongly on Tdet, ranging from 300 to 800 mA at 5 VDC.
Input Range	+4 V to +5.5 V (0.4 to 0.7 A typical).
Initial Transient	2 A for <100 ns

Auxiliary Inputs/Output	
The connectors bring out logic signals which are not required for the primary use of the PX5: acquiring spectra and transmitting them over the serial interface. These are generally “low level” logic signals associated with each pulse processed by the PX5; used for synchronizing the PX5 data acquisition to external hardware and for direct counter/timer outputs from the PX5. The signals are described below.	
Single Channel Analyzers	8 SCAs, independent software selectable LLDs and ULDs, LVCMOS (3.3V)

	level (TTL compatible)
Digital Outputs	Two independent outputs, software selectable between 8 settings including INCOMING_COUNT, PILEUP, MCS_TIMEBASE, etc. LVCMOS (3.3V) levels (TTL compatible).
Digital Inputs	Two independent inputs, software selectable for MCA_GATE, EXTERNAL_COUNTER
Analog Output	Used to display pulses for diagnostic purposes, e.g. finding noise sources or optimizing settings. Software selectable to show shaped output, ADC input, etc., to assist in debugging or optimizing configurations.
Digital Oscilloscope	Displays oscilloscope traces on the computer. Same display as analog output.

Power	
Nominal Input:	+5 VDC at 500 mA (2.5 W) typical. Current depends strongly on T_{det}, ranging from 300 to 800 mA at 5 VDC
Input Range:	+4 V to +5.5 V (at 0.25 to 0.18 A typical)
Initial transient:	2 A for <100 μsec
Power Source:	External supply

Physical	
Dimensions	6.5” x 5.5” x 1.5” / 165 x 135 x 40 mm
Weight	1.6 lbs / 750 g

General and Environmental	
Operating temperature	-40 °C to +85 °C
Warranty Period	1 Year
Typical Device Lifetime	5 to 10 years, depending on use
Storage and Shipping	Long term storage: 10+ years in dry environment Typical Storage and Shipping: -40 °C to +85 °C, 10 to 90% humidity non condensing
Compliance	RoHS Compliant
	TUV Certification Certificate #: CU 72072412 01 Tested to: UL 61010-1: 2004 R7 .05 CAN/CSA-C22.2 61010-1: 2004

Customization

Amptek, Inc. provides many tailored configurations on an OEM basis and has designed the PX5 to be easily customized. This can include interfacing to external hardware (e.g. synchronizing with an external source or controlling external hardware), adding onboard processing, adding special purpose counters, etc. The mechanical detector mounting configuration has been customized to fit into particular sensor assemblies. The PX5 has been configured to utilize other detectors, such as proportional counters or other solid state detectors. Please contact Amptek for more details.

4 ELECTRICAL INTERFACES

4.1 ELECTRICAL SPECIFICATIONS

4.1.1 Absolute Maximum Ratings

Operating Temperature -40°C to +85°C

Power Supply Voltage +6.0 VDC

Analog Input +6.0 to – 6.0 V

NOTICE: Stresses above those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only. Performance at these levels is not implied. Exposure to the conditions of the maximum ratings for an extended period may degrade device reliability.

4.1.2 DC Characteristic

USB

- The USB interface follows the USB 2.0 Full Speed (12 MBPS) specifications.
- The USB transceiver is internal to the C8051F340 from Silicon Laboratories. If technical specifications are required, please refer to the Silicon Laboratories website.

RS-232	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
RX input range		-25		+25	V	
RX threshold low		0.6	1.2		V	
RX threshold high			1.5	2.4	V	
RX hysteresis			0.5		V	
RX input resistance		3	5	7	KΩ	
TX voltage swing		+/- 5	+/- 5.4		V	3 KΩ to ground
TX output resistance		300	10 M		Ω	Unpowered
TX short-circuit current				+/- 60	mA	
baud rate		57.6		115.2	Kbaud	
baud rate accuracy				±1.5%		

- The RS232 interface uses only RXD/TXD lines (no hand-shaking).
- The transceiver is a MAX3227. Please refer to the MAXIM data sheet for further specifications.

AUX OUT						
Output High Voltage	V_{OH}	3.0 1.8	3.3		V V	Typ: No load Min: I_{OH} = -100 μA Min: I_{OH} = -16 mA
Output Low Voltage	V_{OL}		0.0	0.1 1.2	V	Typ: No load Min: I_{OH} = 100 μA Min: I_{OH} = 16 mA
Output Resistance	R_{OUT}		50		Ω	
AUX IN						
Input Voltage		0		5.5	V	
Positive-going Input Threshold	V_{T+}	1.4		2.35	V	
Negative-going Input Threshold	V_{T-}	0.7		1.45	V	
Input Resistance	R_{IN}		100		KΩ	
SCA OUT						
Output High Voltage	V_{OH}	2.9 2.0	3.3		V V	Typ: No load Min: I_{OH} = -100 μA Min: I_{OH} = -12 mA
Output Low Voltage	V_{OL}		0.0	0.2 1.0	V	Typ: No load Max: I_{OH} = 100 μA Max: I_{OH} = 12 mA
Output Resistance	R_{OUT}		47		Ω	

I/O 0 – I/O 3						
Output High Voltage	V_{OH}		3.3		V	
Output Low Voltage	V_{OL}		0		V	
	I_{OH}	30		300	µA	V_{OH} = GND
	I_{OL}	10	25		mA	V_{OL} = 1V

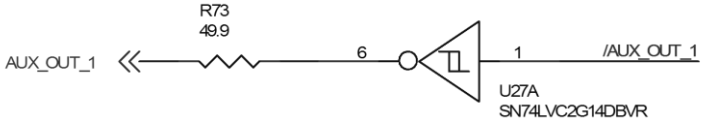
- The AUX OUT lines are the output of a 74LVC2G14 (V_{dd}=3.3V) with 50 Ω series resistance.
- The AUX IN lines are input to a 74LVC2G14 (V_{dd}=3.3V) with 100 kΩ to ground.
- The I/O lines are connected to a MAX7328 (V_{dd}=3.3V), which are open-drain with a weak pull-up.

ANALOG IN						
Input Range Input Impedance	V_{IN}	+4.5 90	-4.5		V MΩ	Standard configuration (no attenuator)
ADC IN						
Range	V_{ADC}	+2.0	0		V	Measured at TP16, AMP3OUT
ANALOG OUT						
Output Range Output Impedance	V_{DAC}	+1.0 499	0		V Ω	

4.2 AUXILIARY INPUT AND OUTPUTS

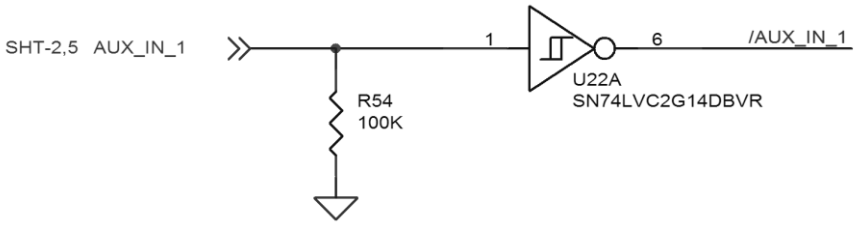
AUX_OUT_1 and _2

- Each of these two lines can be configured, via software, to output any one of several logic signals in the FPGA. These logic signals are associated with pulses processed by the FPGA.
- The pulse timing and duration depends on which output is commanded.
- AUX_OUT_1 is connected to the Interconnect (J5), to the auxiliary connector (J6), and can be jumpered to the stereo jack (J10). AUX_OUT_2 is only connected to the auxiliary connector (J6).



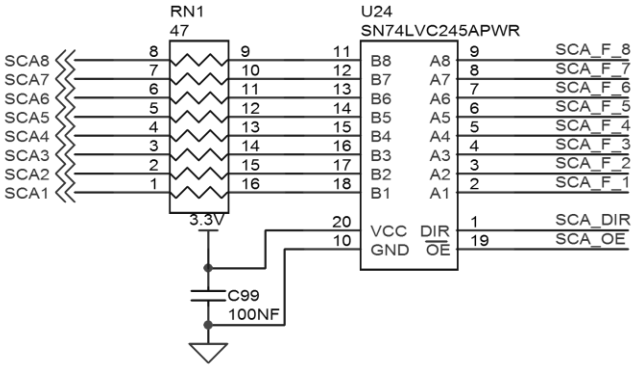
AUX_IN_1 and _2

- Each of these two lines can be configured, via software, to input any one of several logic signals in the FPGA. These logic signals are associated with pulses processed by the FPGA.
- AUX_IN_1 is connected to the Interconnect (J5), to the auxiliary connector (J6), and can be jumpered to the stereo jack (J10). AUX_IN_2 is only connected to the auxiliary connector (J6).

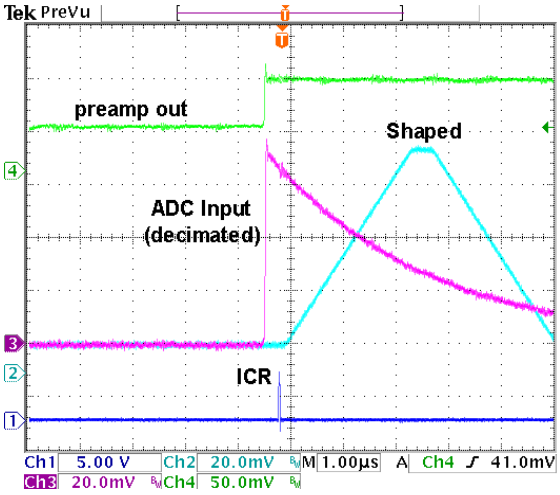


Single Channel Analyzers (SCAs)

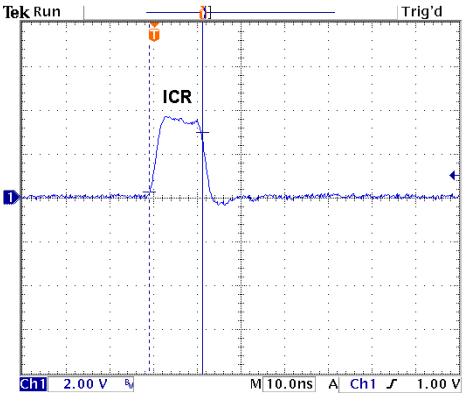
- Each of the eight SCAs has an independently assignable LLD and a ULD. If the shaped pulse peaks within the range of an SCA, between its LLD and ULD, then a logic signal is output.
- These output pulses are 100 nsec wide (the ability to select longer pulse widths is a future enhancement.)



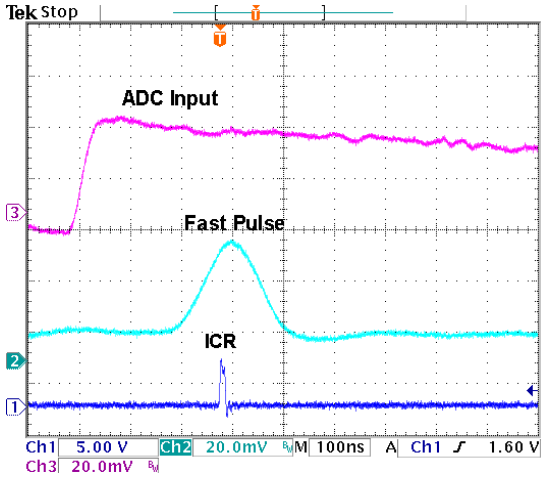
4.3 TIMING OF AUXILIARY INPUTS AND OUTPUTS



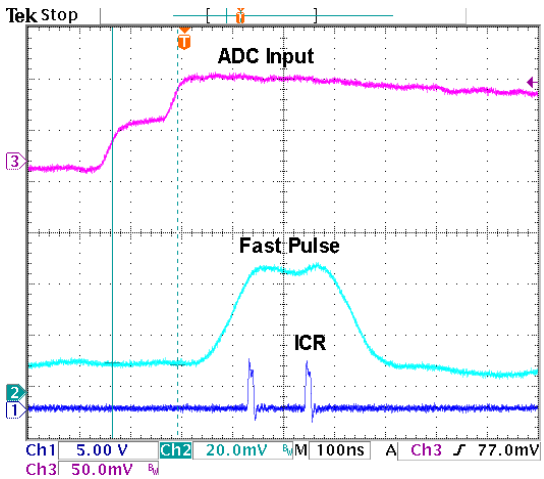
Preamp output, ADC input, shaped pulse (T_{peak} of 2.4 µsec and T_{flat} of 0.8 µsec) and ICR (logic pulse indicating that a fast channel pulse occurred). Note that (1) the shaped pulse begins to rise after actual event (due to delays in the digital pipeline), and (2) ICR occurs when the shaped pulse begins to rise.



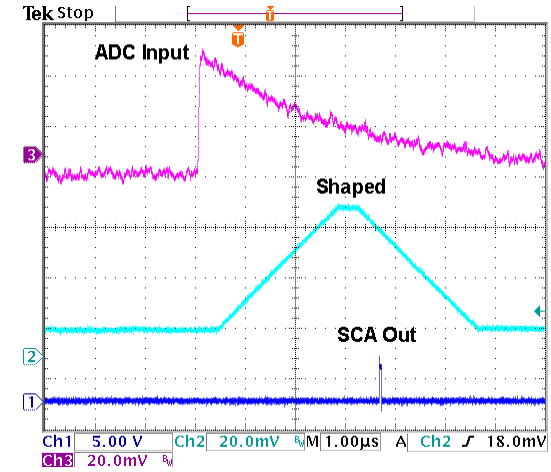
ICR – Measured by scope probe, 10 MΩ, 15 pF, and 300 MHz scope. One clock (12.5 nsec) wide.



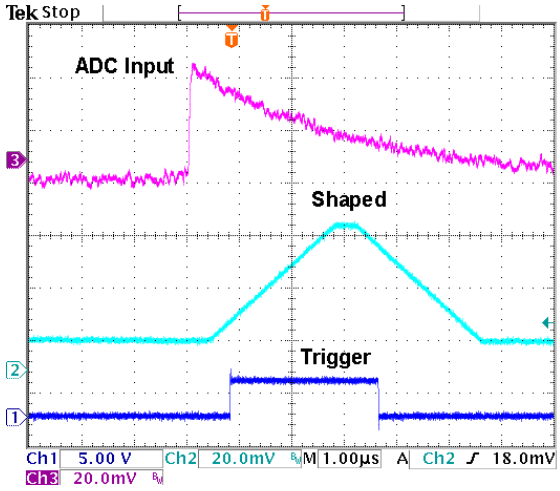
ADC input, fast channel pulse (T_{peak} of 0.1 µsec) and ICR. Similar to plot at left but at high time resolution.



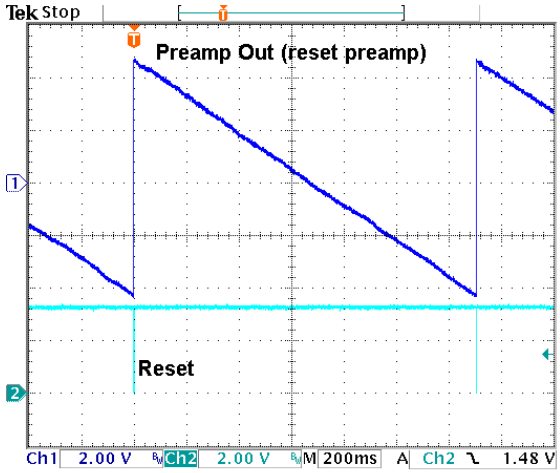
ADC input, fast channel pulse, and ICR. Similar to plot above but shows ability of fast channel to identify pulses separated by 120 nsec.



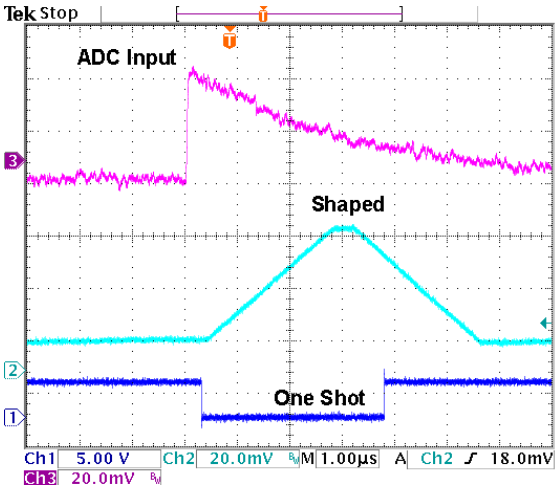
SCA output. Occurs just after the shaped pulse has begin to fall.



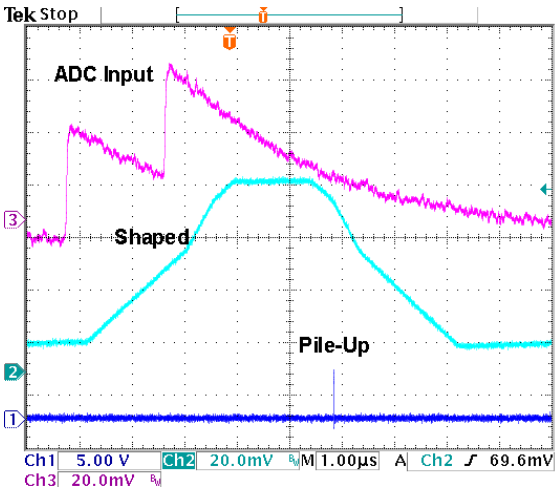
Trigger. Shows when the DPP is looking for the peak of a pulse. Falling edge indicates a peak has been found.



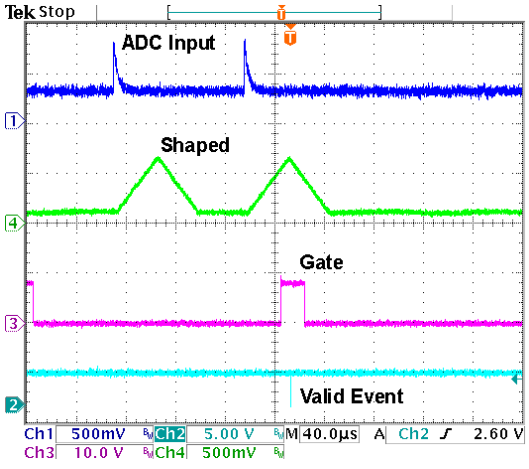
Detector Reset. Shows when the DPP detected a reset signal in the preamplifier. The lockout period is the width of the reset signal.



One-Shot. Shows when the DPP is looking for possible pile-up. Triggered by the fast channel.



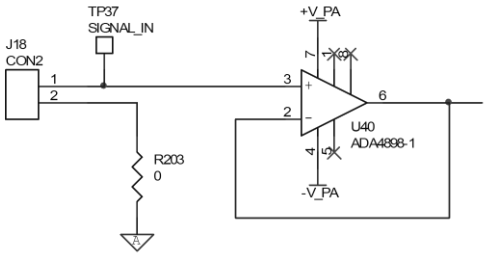
Pile-Up. Shows when pile-up was detected. Generated at the end of the final event's one-shot signal.



Gate. This is an INPUT by which external logic can select pulses to be accepted into the spectrum. If GATE is TRUE at the time the peak is detected (the falling edge of trigger), the event is accepted. In this figure, the second pulse is accepted, not the first.

4.4 ANALOG INPUT

- Shown below is a simplified schematic of the analog input. There are several jumpers on the board which permit this front end to be reconfigured for use with a variety of different detectors and preamplifiers. Contact Amptek to discuss these options



- V_PA can be set to +/-5V or to +/- 8.5V. The input amplifier's output voltage swing is +/- 3.3V or +/- 6.8V, depending on V_PA. The absolute max is +11 to -11V.

4.5 POWER SUPPLY ARCHITECTURE

Figure 4-1 is a block diagram of the power supplies in the PX5.

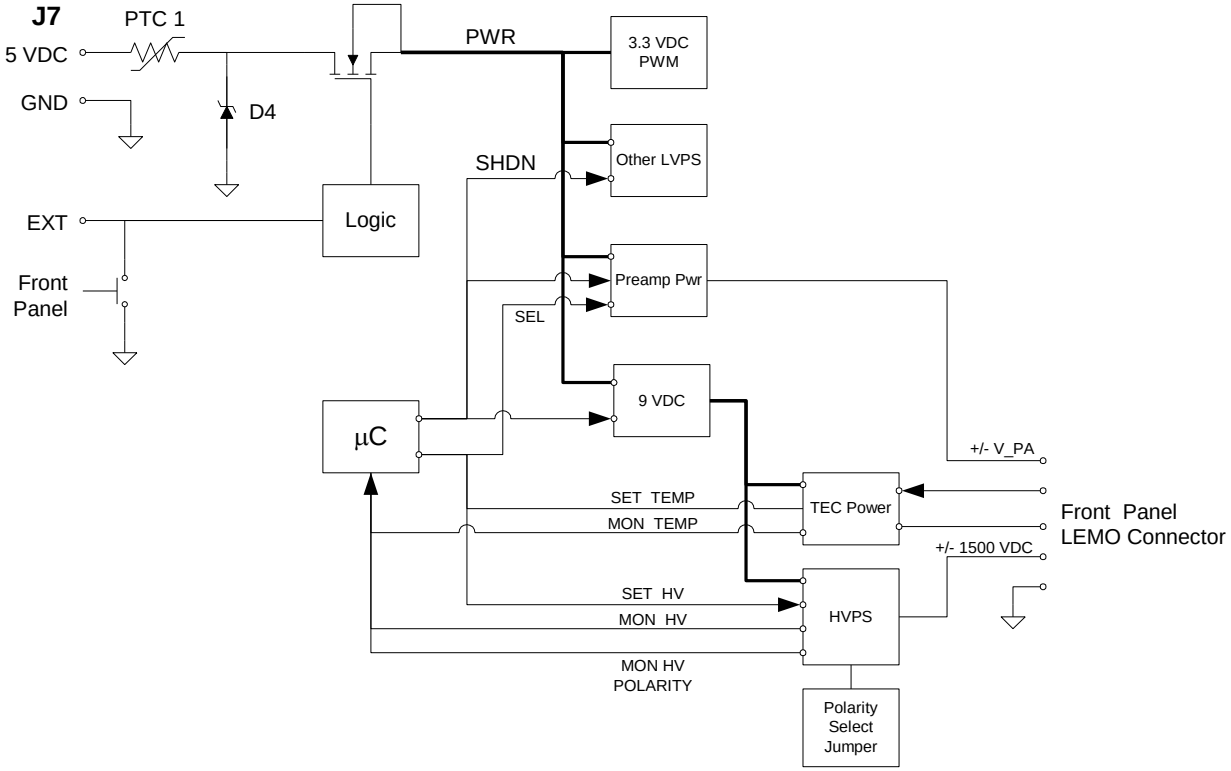


Figure 4-1. Block diagram of the power supplies in the PX5.

Some key points of the overall architecture are as follows:

- The input power is nominally +5 VDC (4 V to 5.5 V acceptable).
- Reverse polarity protection is provided by PTC1 and D4. There is no over or under voltage protection.
- F1 is a polyfuse, i.e. a resettable fuse. It goes to a high impedance with very high current but returns to low impedance after power is removed. It does not need replacing after use.

- The front panel switch is a momentary switch. When the switch is depressed, the edge is detected by the logic and the MOSFET switches open or closed. The EXT line on J3 permits the user to switch the power off or on remotely.
- When power is applied, the 3.3V supply in the turns on and the digital circuitry is powered. When the PX5 is configured, the microcontroller turns on its low voltage supplies. Based on the configuration choices, the preamp power, 9VDC supply, and the HV and cooler supplies may be enabled.
- There are several different pulse width modulated power supplies used in the PX5. Nominal switching frequencies are >1 MHz, except for the HVPS, which uses about 60 kHz.

4.5.1 High voltage Power Supply

WARNING: Using the wrong polarity will destroy the detector and will NOT be covered under warranty. Always check that the correct HV polarity is set before turning on the PX5.

- The high voltage power supply can provide positive or negative polarity, at voltages up to 1500 VDC and currents up to 30 μA. It is suitable for solid state detectors.
- The polarity is changed by a jumper on the bottom of the PX5. To change polarity, turn off the PX5, unthread the two screws, remove the jumper, turn it around, carefully re-insert it, then thread the screws. The polarity is indicated by the line on the jumper. The polarity is also indicated by the color of the LED ring on the front panel power switch: green (red) for positive (negative).
- The polarity is set in hardware. There is also a polarity flag in software. The PX5 μC compares the hardware jumper with the software flag. If they do not agree, then HV supply is disabled. To enable, change one or the other to make them agree.
- The magnitude of the power supply is controlled by a DAC so can be commanded in software to 1500 VDC. The output is monitored by an ADC (it typically reads a few volts when the HV is turned off).
- The HV supply has a series resistance of 0.5 kΩ for current limiting.

WARNING: Using the wrong polarity will destroy the detector and will NOT be covered under warranty. Always check that the correct HV polarity is set before turning on the PX5.

4.6 TEC SUPPLY

- The TEC supply provides closed loop temperature control for the thermoelectric cooler in Amptek's X-ray detectors. The forward voltage across a diode (1N914) inside the detector hybrid is used to measure the temperature. The TEC supplies up to 3.6V to drive the two stage cooler.
- The cooler can typically provide a temperature differential of up to 75-80^{o}C. At room temperature, 22^{o}C or 295K, the cooler can typically reach 220K. At elevated temperatures, the detector will be warmer. Note that ΔT is defined relative to the stud on the back of the detector. If this does not have a good heat sink, then the detector will be warmer.

4.6.1 Preamp Supplies

- The preamp power supplies can be configured in software for +/- 5VDC or +/- 8.5 VDC. Amptek's XR100 preamplifiers require +/-8.5 VDC for proper operation while the PA210/PA230 preamplifiers require +/- 5 VDC.
- The 5VDC setting is appropriate for Amptek's PA210 family of preamplifiers. NOTE: THESE PREAMPS CAN BE DAMAGED IF 8.5 VDC IS APPLIED.
- Note: The preamp power supply also provides power to the front end analog circuitry in the PX5. If preamp power is disabled, then the front end of the PX5 is not powered and hence it does not work.

4.6.2 Custom Supplies

- Amptek has designed the PX5 to accommodate custom power supplies for various detectors. For example, a custom module for HPGe detectors provides +/- 5 kV bias voltage and provides +/- 12 VDC and +/- 24 VDC power for the preamplifiers.
- Please contact Amptek to discuss custom options.

5 CONNECTORS

Power

Mates with a center positive 5.5 mm x 2.1 mm power plug.

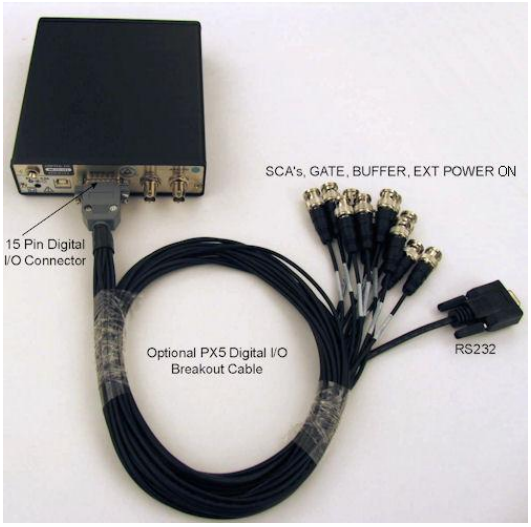
Pin #	Name
1	VIN (+5 V DC)
2	GND

Auxiliary

Digital I/O: 15 pin D connector (female)

Mates with Amptek breakout cable assembly

Pin #	Name	Pin #	Name
1	Gnd	9	SCA 8 Out
2	RS232 - TX	10	External Power On
3	RS232 -RX	11	SCA 7 Out
4	SCA 6 Out	12	SCA 1 Out
5	SCA 5 Out	13	SCA 2 Out
6	Gnd	14	SCA 3 Out
7	Aux 3	15	SCA 4 Out
8	Aux 4		



Ethernet

Standard Ethernet connector (RJ-45)

USB

Standard USB ‘mini-B’ jack.

Analog In

Standard BNC connector.

Pin	Signal	Comment
1	Input	IN+ of input amplifier
2	GND	Can jumper to IN- of amplifier

XR100 Power

6-pin Lemo Connector: Part# ERA.1S.306.CLL
Mates with Part# FFA.1S.306.CLAC57

1	Temperature
2	Bias (up to ±1500V) **WARNING: Using the wrong polarity will destroy the detector and will NOT be covered under warranty. Always check that the correct HV polarity is set before turning on the PX5.**
3	-8.5 or -5 VDC
4	+8.5 or +5 VDC
5	Cooler - (grounded)
6	Cooler +
Ground on shield	

High Voltage Jumper

WARNING: Using the wrong polarity will destroy the detector and will NOT be covered under warranty. Always check that the correct HV polarity is set before turning on the PX5.

The PX5 can produce both negative and positive high voltage. The polarity is set by the jumper seen below. Amptek Si-PIN and CdTe detectors require positive high voltage. Using negative HV will destroy the Si-PIN and CdTe and will not be covered under warranty. Amptek silicon drift detectors (SDD) require negative high voltage. Using positive HV will destroy the SDD and will not be covered under warranty.

PX5 high voltage jumper set to positive for Si-PIN or CdTe detector.

PX5 high voltage jumper set to negative for silicon drift detector (SDD)

WARNING: Using the wrong polarity will destroy the detector and will NOT be covered under warranty. Always check that the correct HV polarity is set before turning on the PX5.

6 SOFTWARE

Please see the "WINUSB Driver Installation Instructions" and the "PX5 Quick Start Guide" for instructions on installing the USB driver and the DPPMCA software.

6.1 INTERFACE SOFTWARE

DPPMCA Software

The DP5 can be controlled by the Amptek DPPMCA display and acquisition software. This software completely controls and configures the DP5, and downloads and displays the data. It and supports regions of interest (ROI), calibrations, peak searching, and so on.

DPP SDK

The PX5 comes with a Software Developer's Kit from which the user can write custom code to control the PX5 for custom applications or to interface it to a larger system. Examples are provided in VB and C++.

VB Demonstration Software

The VB demonstration software runs on a personal computer and permits the user to set the PX5 parameters, to start and stop data acquisition, and to save data files. It is provided with source code and can be modified by the user. This software is intended as an example of how to manually control the PX5 through either the USB or RS-232 interface using the most basic calls.

6.2 EMBEDDED SOFTWARE

The embedded software is responsible for controlling the pulse processing, controlling the MCA, carrying out some data processing, and interfacing with the personal computer. Firmware updates will be released by Amptek and can be uploaded in the field by the user.

7 TROUBLESHOOTING AND ADVICE

7.1 GROUNDING IS CRITICAL TO PERFORMANCE!

- Amptek **strongly** recommends using a single point ground for the system. There is a banana jack on the back of the PX5 for this purpose. Ground currents flowing through multiple connections, through a lab bench, etc. often induce noise.
- We have observed several laptops in which the AC adapter introduced ground noise. In these cases better performance was found by (1) using a 3-prong to 2-prong adapter on the power supply of any notebook computer and (2) making a separate ground connection to the DPP. Note that the DPP's AC/DC supply is isolated.

7.2 CONFIGURATION SUGGESTIONS

- The DPPMCA software contains default configuration settings for Amptek's detectors. These may not be optimum for your application but should provide a good starting point. In DPPMCA, choose the "Acquisition Setup" toolbar button, then select the appropriate configuration from the drop-down.
- The "fast" and "slow" thresholds have a significant impact on performance. After setting other configuration options it is best to reset the thresholds using the "Tune Slow/Fast" button on DPPMCA toolbar. If the auto tune fails follow the instructions below.
- The Fast and Slow Thresholds can be adjusted manually. First turn off PUR. Then click the cursor to channel 1 and press F8. This will set the Slow Threshold (LLD) to channel 1. This will show the noise of the system. Click the cursor just to the right of the noise and then press F8. Press the "A" key to clear. There should be no counts accumulating. Now put the device into "Delta" mode by clicking the Delta button on the toolbar. Open the DPP Properties and go to the Shaping page. Adjust the Fast Threshold until 5 to 15 counts per second appear in the Input Counts in the right-hand Info Panel. Now turn on PUR and click OK. Click the Delta button to go back to normal MCA mode and put the source back in front of the detector. The Input Counts should slightly exceed the Total Counts at low count rate.
- The baseline restoration setting can have a significant impact on performance. It stabilizes the spectrum over count rate but also suppresses low frequency noise and interference. Turning BLR parameters ON will improve resolution, peak stability and suppress spectral artifacts. Amptek recommends always using BLR. For most applications with Amptek detectors a BLR setting of DN 3 UP 0 works well.

8 SYSTEM BLOCK DIAGRAM

The block diagram below shows a typical PX5 application with an Amptek AXR detector and XR100 preamplifier. This outlines the signal flow and the power supply and ground connections.